DEDICATED MCU FAMILY

FOR TELEPHONE SET APPLICATIONS

DATABOOK

1st EDITION

JANUARY 1994

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

SGS-THOMSON's extensive dedicated telephone set product range can meet virtually all needs of developers and producers of low, mid and high end telephone sets, answering machines and related applications.
Complementing our devices for line protection, interface and speech, tone and ring drivers, is SGS-THOMSON's dedicated microcontroller product line for telephone sets. Performing the central control functions and user features of modern feature phone telephone sets, the microcontroller range has been expanded to cover all model requirements: from basic telephones with Last Number Redial and 3 to 10 stored numbers - to Hands Free telephones and feature phones - to integrated telephone answering machine controllers.

Since each microcontroller device is applicable for more than one area of use, the entire product line is covered in the Telephone Set ICs Databook and Application Manuals.

SGS-THOMSON's microcontrollers have two roots. Firstly, the successful non-dedicated families for general applications, and secondly the Company's capabilities in non-volatile memory technologies. With experience gained from a long history of involvement in telephone set applications, SGS-THOMSON has developed two families of dedicated microcontrollers and a dedicated DSP device, each with integrated features making them attractive and cost-effective system solutions.

These integrated functions offer features such as: on-chip EEPROM for number storage and user preferences; I/O port wakeup functions for low power operation; on-chip digital to analog converters for analog controls; voice compression and synthesis, tone and DTMF detectors (DSP based); and optimized interfaces to SGS-THOMSON dedicated telephone set products. The microcontroller-based system complements and adds to the dedicated functions the flexibility that only a microcontroller-based system can offer.

ST62 8-bit MCUs with ADC and SPI

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	I/O	TIMER/ WDOG	TEMP RANGE	OP. VOLTAGE	PACKAGE	EMULATING DEVICES
ST6260	4K	128	128	13	2/1	-40,+85°C	3.0V-6.0V	PDIP20,PSO20	-
ST6294	4K	128	128	21	2/1	-40,+85°C	3.0V-6.0V	PDIP28,PSO28	ST62E94

ST72 8-bit MCUs

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	I/O	TIMER/ WDOG	TEMP RANGE	OP. VOLTAGE	PACKAGE	EMULATING DEVICES
ST7291	16K	256	-	19	1/-	0,+70°c	3.0V-5.5V	PDIP28,PSO28	-
ST7293	3.3K	128	128	22	1/1	-25,+85°C	2.5V-5.5V	PDIP28,PSO28	ST72E94
ST7294	6K	224	256	22	1/1	-25,+85°C	2.5V-5.5V	PDIP28,PSO28	ST72E94

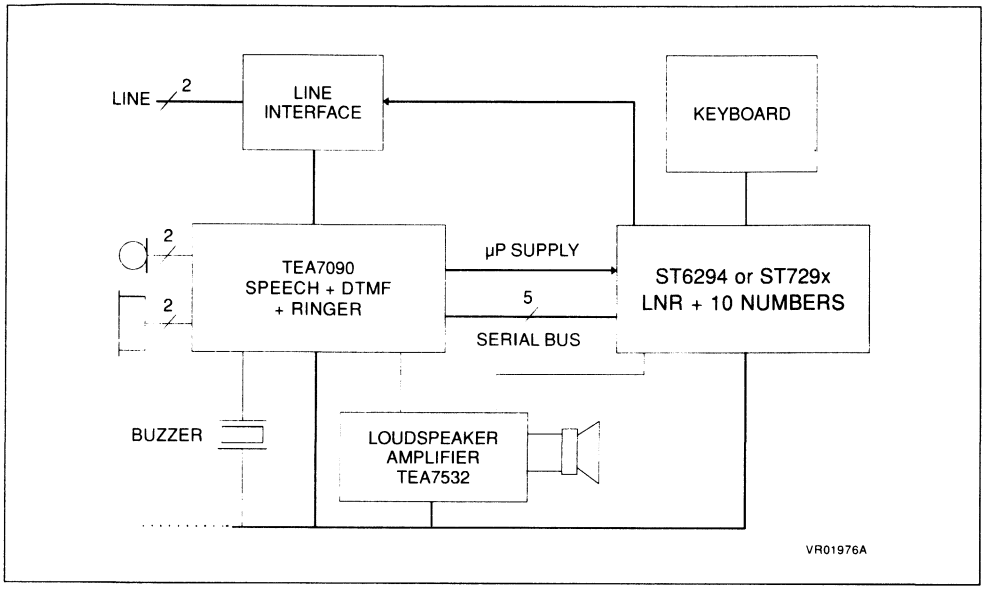
ST62 8-bit OTP/EPROM MCUs

DEVICE	EPROM (Bytes)	OTP ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	I/O	TIMER/ WDOG	TEMP RANGE	OP. VOLTAGE	PACKAGE	EMULATED DEVICES
ST62E94	4K	-	128	128	21	2/1	0,+70°c	3.0V-6.0V	CDIP28W	ST6294
ST62T94	-	4K	128	128	21	2/1	-25,+85°C	3.0V-6.0V	PDIP28 PSO28	ST6294

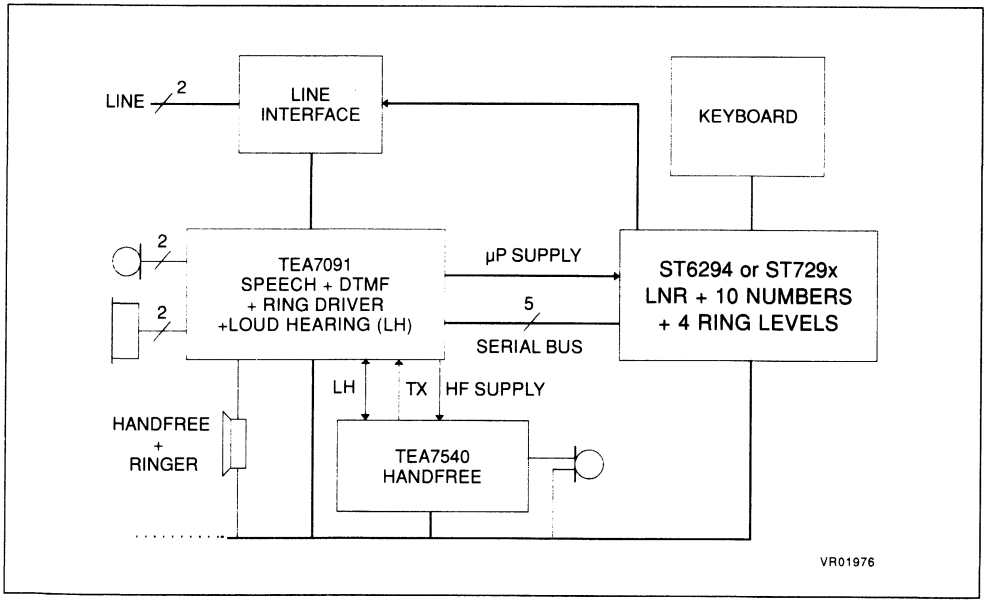
ST72 8-bit OTP/EPROM MCUs

DEVICE	EPROM (Bytes)	OTP ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	I/O	TIMER/ WDOG	TEMP RANGE	OP. VOLTAGE	PACKAGE	EMULATED DEVICES
ST72E94	6K	-	224	256	22	1/1	0,+70°c	3.0V-5.5V	CDIP28W	ST7294 ST7293
ST72T94	-	6K	224	256	22	1/1	-25,+85°C	3.0V-5.5V	PDIP28 PSO28	ST7294 ST7293

Middle-range Telephone Set With Ringer, 10 Repertory Numbers and Loudspeaker



Middle-range Telephone Set With Ringer, 10 Repertory Numbers and Handfree.



8 Bit MCUs

16/32 Bit DSP

8 Bit MCUs

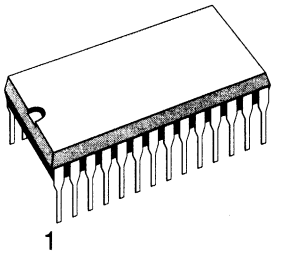
SGS-THOMSON MICROELECTRONICS

ST6260
ST6265

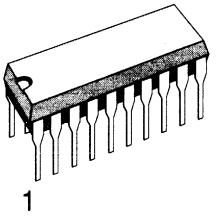
8-BIT HCMOS MCUs WITH A/D CONVERTER, EEPROM & AUTO-RELOAD TIMER

PRELIMINARY DATA

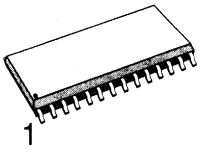
- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User ROM: 3868 bytes
- Data ROM: User selectable size (in program ROM)
- Data RAM: 128 bytes
- EEPROM: 128 bytes
- PDIP20, PSO20 (ST6260) packages
- PDIP28, PSO28 (ST6265) packages
- 13/21 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- 6/8 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer1)
- 8 bit auto-reload timer with 7-bit programmable prescaler (AR Timer)
- Digital Watchdog
- 8 bit A/D Converter with up to 7 (ST6260) and up to 13 (ST6265) analog inputs
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator (Quartz Crystal or Ceramic)
- Power-on Reset
- One external not maskable interrupt
- 9 powerful addressing modes
- The development tool of the ST626x microcontrollers consists of the ST626x-EMU emulation and development system connected via a standard RS232 serial line to an MS-DOS Personal Computer



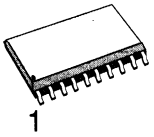
PDIP28



PDIP20



PSO28



PSO20

(Ordering Information at the end of the datasheet)

Figure 1. ST6260 Pin Configuration

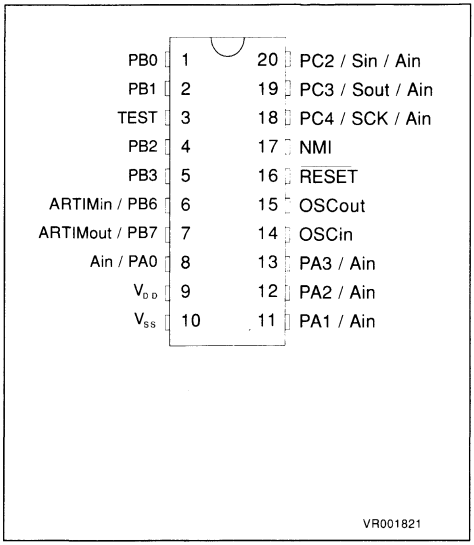


Figure 2. ST6265 Pin Configuration

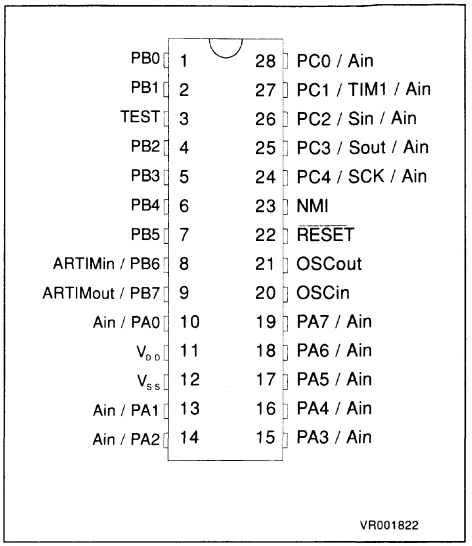
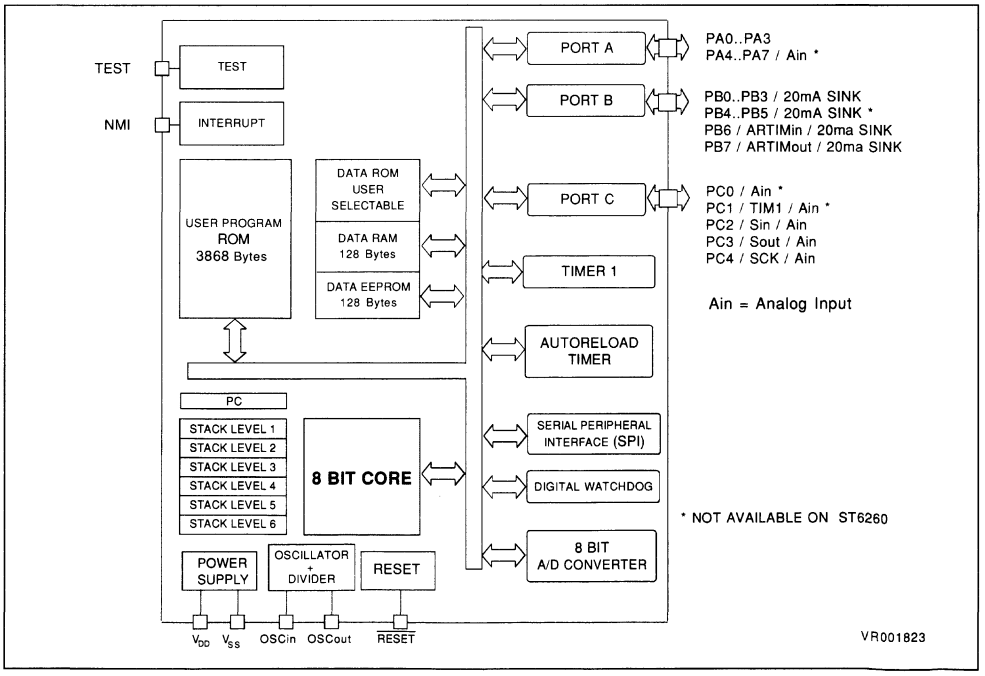


Figure 3. ST6260,65 Block Diagram



GENERAL DESCRIPTION

The ST6260 and ST6265 microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells). The macrocells of the ST6260 and ST6265 are: the Timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer1), the 8-bit Auto-reload Timer with 7 bit programmable prescaler (AR Timer), the 8-bit A/D Converter with up to 7 (ST6260) and up to 13 (ST6265) analog inputs (A/D inputs are alternate functions of I/O pins), the Digital Watchdog (DWD) and an 8-bit Serial synchronous Peripheral Interface (SPI). In addition, these devices offer 128 bytes of EEPROM for non volatile data storage.
ST6260 and ST6265 are well suited for automotive, appliance and industrial applications. The ST62E60 and ST62E65 EPROM versions are available for prototypes and low-volume production; also OTP versions are available.

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The frequency at OSCin and OSCout is internally divided by 1, 2 or 4 by a software controlled divider.The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST. The TEST must be held at VSS for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous interrupt applying an external not maskable interrupt to the MCU. The NMI is falling edge sensitive. It is provided with an on-chip pull-up resistor and Schmitt trigger characteristics.

PC1/TIM1/Ain. This pin can be used as a Port C I/O bit, as Timer 1 I/O pin or as analog input for the on-chip A/D converter. This pin is available only on the ST6265 (28 pin version). If programmed to be the Timer 1 pin, in input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time out occurs.
To use this pin as Timer 1 output a dedicated bit in the TIMER 1 Status/Control Register must be set. To use this pin as input pin the I/O pin has to be programmed as input. The analog mode should be programmed to use the line as an analog input.

PB6/ARTIMin, PB7/ARTIMout. These pins are either Port B I/O bits or the Input and Output pins of the Auto-reload Timer. To be used as timer input function PB6 has to be programmed as input with or without pull-up. A dedicated bit in the AR TIMER Mode Control Register sets PB7 as timer output function.

PA0-PA7. These 8 lines are organized as one I/O port (A). PA4-PA7 are not available on ST6260 (20 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input, open-drain or push-pull output.

PB0-PB3, PB4, PB5. These 6 lines are organized as one I/O port (B). PB4, PB5 are available only on the ST6265 (28 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED and TRIAC driving. The reset configuration of PB0-PB3 can be selected by mask option (pull-up or high impedance).

PC0-PC4. These 5 lines are organized as one I/O port (C). PC0 and PC1 are not available on ST6260 (20 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input for the A/D converter, open-drain or push-pull output. PC2-PC4 can also be used as respectively Data in, Data out and Clock I/O pins for the on-chip SPI to carry the synchronous serial I/O signals.

ST62xx CORE

The core of the ST62xx Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control busses. The in-core communication is arranged as shown in Figure 5; the controller being externally linked to both the reset and the oscillator, while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes through the control registers.

Registers

The ST62xx Family core has six registers and three pairs of flags available to the programmer. They are shown in Figure 4 and are explained in the following paragraphs.

Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator is addressed in the data space as RAM location at address FFh. Accordingly the ST62xx instruction set can use the accumulator as any other register of the data space.

Figure 4. ST62xx Core Programming Model

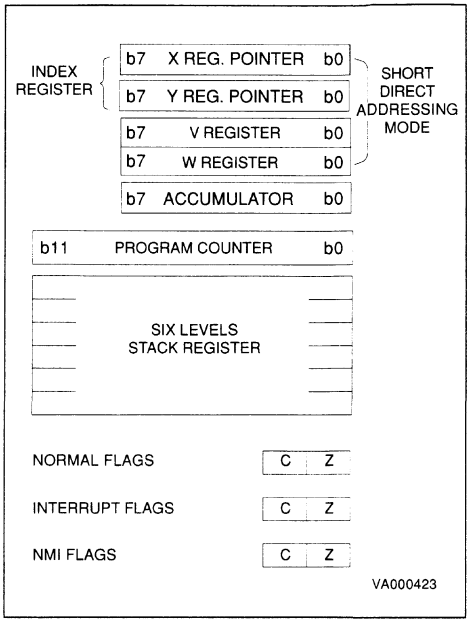
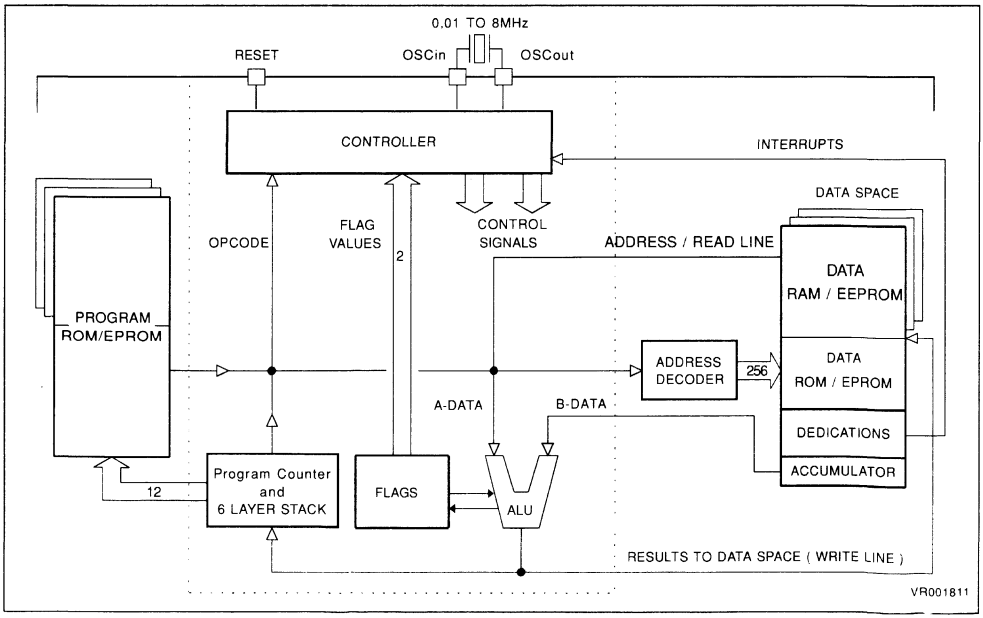


Figure 5. ST62xx Core Block Diagram



ST62xx CORE (Continued)

Indirect Registers (X, Y). These two indirect registers are used as pointers to the memory locations in the data space. They are used in the register-indirect addressing mode. These registers can be addressed in the data space as RAM locations at addresses 80h (X) and 81h (Y). They can also be accessed with the direct, short direct, or bit direct addressing modes. Accordingly, the ST62xx instruction set can use the indirect registers as any other register of the data space.

Short Direct Registers (V, W). These two registers are used to save one byte in short direct addressing mode. These registers can be addressed in the data space as RAM locations at addresses 82h (V) and 83h (W). They can also be accessed with the direct and bit direct addressing modes. Accordingly, the ST62xx instruction set can use the short direct registers as any other register of the data space.

Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next ROM location to be processed by the core. This ROM location may be an opcode, an operand, or an address of operand. The 12-bit length allows the direct addressing of 4096 bytes in the program space. Nevertheless, if the program space contains more than 4096 locations, the further program space can be addressed by using the Program Bank Switch register.
The PC value is incremented, after it is read the address of the current instruction. To execute relative jumps the PC and the offset are shifted through the ALU, where they will be added, and the result is shifted back into the PC. The program counter can be changed in the following ways:

- JP (Jump) instruction . . . PC= Jump address
- CALL instruction . . . . PC= Call address
- Relative Branch Instructions. PC= PC ± offset
- Interrupt . . . . . PC= Interrupt vector
- Reset . . . . . PC= Reset vector
- RET & RETI instructions . PC= Pop (stack)
- Normal instruction . . . . PC= PC + 1

Flags (C, Z)

The ST62xx core includes three pairs of flags that correspond to 3 different modes: normal mode, interrupt mode and Non-Maskable-Interrupt-mode. Each pair consists of a CARRY flag and a ZERO flag. One pair (CN, ZN) is used during normal operation, one pair is used during the interrupt mode (CI, ZI) and one is used during the not-maskable interrupt mode (CNMI, ZNMI).

The ST62xx core uses the pair of flags that correspond to the actual mode: as soon as an interrupt (resp. a Non-Maskable-Interrupt) is generated, the ST62xx core uses the interrupt flags (resp. the NMI flags) instead of the normal flags. When the RETI instruction is executed, the normal flags (resp. the interrupt flags) are restored if the MCU was in the normal mode (resp. in the interrupt mode) before the interrupt. It should be observed that each flag set can only be addressed in its own routine (Not-maskable interrupt, normal interrupt or main routine). The flags are not cleared during the context switching and so remain in the state they were at the exit of the last routine switching.

The Carry flag is set when a carry or a borrow occurs during arithmetic operations, otherwise it is cleared. The Carry flag is also set to the value of the bit tested in a bit test instruction, and participates in the rotate left instruction.

The Zero flag is set if the result of the last arithmetic or logical operation was equal to zero, otherwise it is cleared.

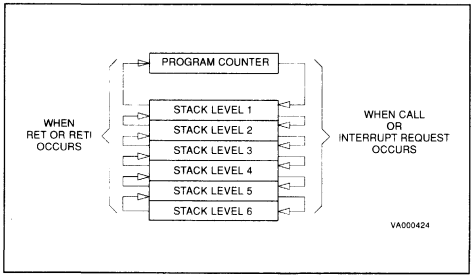
The switching between the three sets of flags is automatically performed when an NMI, an interrupt or a RETI instructions occurs. As the NMI mode is automatically selected after the reset of the MCU, the ST62xx core uses at first the NMI flags.

ST62xx CORE (Continued)

Stack

The ST62xx core includes true LIFO hardware stack that eliminates the need for a stack pointer. The stack consists of six separate 12-bit RAM locations that do not belong to the data space RAM area. When a subroutine call (or interrupt request) occurs, the contents of each level is shifted into the next level while the content of the PC is shifted into the first level (the value of the sixth level will be lost). When a subroutine or interrupt return occurs (RET or RETI instructions), the first level register is shifted back into the PC and the value of each level is popped back into the previous level. These two operating modes are described in Figure 6. Since the accumulator, as all other data space registers, is not stored in this stack the handling of these registers should be performed inside the subroutine. The stack pointer will remain in its deepest position if more than 6 calls or interrupts are executed, so that the last return address will be lost. It will also remain in its highest position if the stack is empty and a RET or RETI is executed. In this case the next instruction will be executed.

Figure 6. Stack Operation



MEMORY SPACES

The MCU operates in three different memory spaces: program space, data space, and stack space. A description of these spaces is shown in the following figures.

Program Space

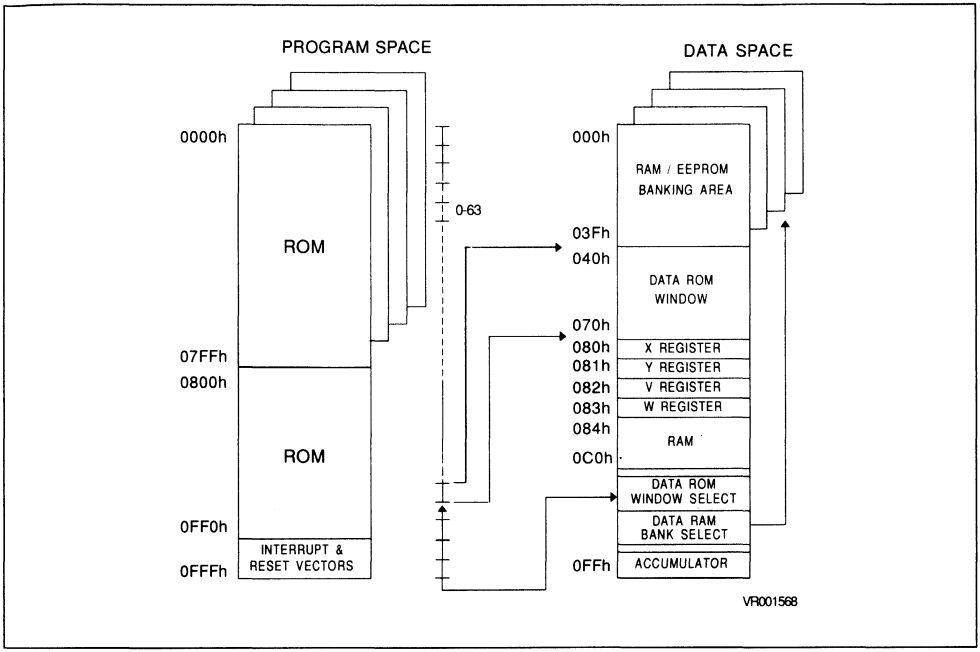
The program space is physically implemented in the ROM memory and includes all the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, the reserved test area and the user vectors. It is addressed by the 12-bit Program Counter register (PC register) and so the ST62xx core can directly address up to 4K bytes of Program Space.

Table 1. ST6260/65 Program ROM Memory Map

Device Address	Description
0000h-007Fh	Reserved
0080h-0F9Fh	User Program ROM 3856 Bytes
0FA0h-0FEFh 0FF0h-0FF7h 0FF8h-0FFBh 0FFCh-0FFDh 0FFEh-0FFFh	Reserved Interrupt Vectors Reserved NMI Vector User Reset Vector

MEMORY SPACES (Continued)

Figure 7. Memory Addressing Description Diagram



MEMORY SPACES (Continued)

Data Space

The instruction set of the ST62xx core operates on a specific space, named Data Space, that contains all the data necessary for the processing of the program. The Data Space allows the addressing of RAM and EEPROM memory, ST62xx core/peripheral registers, and read-only data such as constants and look-up tables.

Data ROM. All the read-only data is physically implemented in the ROM memory in which the Program Space is also implemented. The ROM memory contains consequently the program to be executed, the constants and the look-up tables needed for the program.

The locations of Data Space in which the different constants and look-up tables are addressed by the ST62xx core can be considered as being a 64-byte window through which it is possible to access to the read-only data stored in the ROM memory .

Data RAM/EEPROM. The ST6260/65 offer 128 bytes of data RAM memory and 128 bytes of EEPROM. 64 bytes of RAM are directly addressed in data space in the range 080h-0BFh (static space). The additional RAM and EEPROM are addressed using the banks of 64 bytes located between addresses 00h and 3Fh.

Stack Space

The stack space consists of six 12 bit registers that are used for stacking subroutine and interrupt return addresses plus the current program counter register.

Figure 8. ST6260,65 Data Memory Space

DATA and EEPROM	000h 03Fh
DATA ROM WINDOW AREA	040h 07Fh
X REGISTER	080h
Y REGISTER	081h
V REGISTER	082h
W REGISTER	083h
DATA RAM	084h 0BFh
PORT A DATA REGISTER	0C0h
PORT B DATA REGISTER	0C1h
PORT C DATA REGISTER	0C2h
RESERVED	0C3h
PORT A DIRECTION REGISTER	0C4h
PORT B DIRECTION REGISTER	0C5h
PORT C DIRECTION REGISTER	0C6h
RESERVED	0C7h
INTERRUPT OPTION REGISTER	0C8h*
DATA ROM WINDOW REGISTER	0C9h*
RESERVED	0CAh 0CBh
PORT A OPTION REGISTER	0CCh
PORT B OPTION REGISTER	0CDh
PORT C OPTION REGISTER	0CEh
RESERVED	0CFh
A/D DATA REGISTER	0D0h
A/D CONTROL REGISTER	0D1h
TIMER 1 PRESCALER REGISTER	0D2h
TIMER 1 COUNTER REGISTER	0D3h
TIMER 1 STATUS/CONTROL REGISTER	0D4h
AR TIMER MODE CONTROL REGISTER	0D5h
AR TIMER STATUS/CONTROL REGISTER1	0D6h
AR TIMER STATUS/CONTROL REGISTER2	0D7h
WATCHDOG REGISTER	0D8h
AR TIMER RELOAD/CAPTURE REGISTER	0D9h
AR TIMER COMPARE REGISTER	0DAh
AR TIMER LOAD REGISTER	0DBh
OSCILLATOR CONTROL REGISTER	0DCh*
MISCELLANEOUS	0DDh
RESERVED	0DEh 0DFh
SPI DATA REGISTER	0E0h
SPI DIVIDER REGISTER	0E1h
SPI MODE REGISTER	0E2h
RESERVED	0E3h 0E7h
DATA RAM PAGE REGISTER	0E8h*
RESERVED	0E9h
EEPROM CONTROL REGISTER	0EAh
RESERVED	0EBh 0FEh
ACCUMULATOR	0FFh

* WRITE ONLY REGISTER

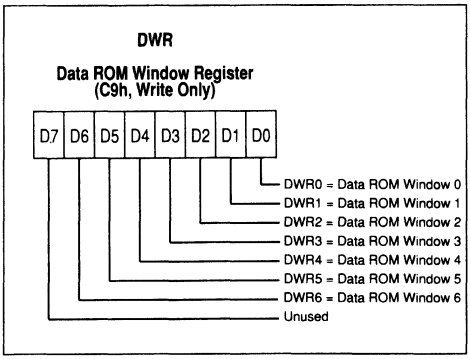
MEMORY SPACES (Continued)

Data Window register (DWR)

The Data ROM window is located from address 040h to address 7Fh in the Data space. It allows the direct reading of 64 consecutive bytes located anywhere in the ROM memory between the addresses 0000h and 1FFFh. All the bytes of the ROM memory can be used to store either instructions or read-only data. Indeed, the window can be moved by step of 64 bytes along the ROM memory in writing the appropriate code in the Write-only Data Window register (DWR register, location C9h).

The DWR register can be addressed like a RAM location in the Data Space at the address C9h, nevertheless it is a write only register that cannot be accessed with single-bit operations. This register is used to move the 64-byte read-only data window (from the 40h address to 7Fh address of the Data Space) up and down the ROM memory of the MCU in steps of 64 bytes. The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 least significant bits of the register address given in the instruction (as least significant bits) and the content of the DWR register (as most significant bits, see Figure 8). So when addressing location 40h of dataspace, and 0 is loaded in the DWR register, the phisycal addressed location in ROM is 00h. The DWR register is not cleared at reset, therefore it must be written to before the first access to the Data ROM window area.

Figure 10. Data ROM Window Register



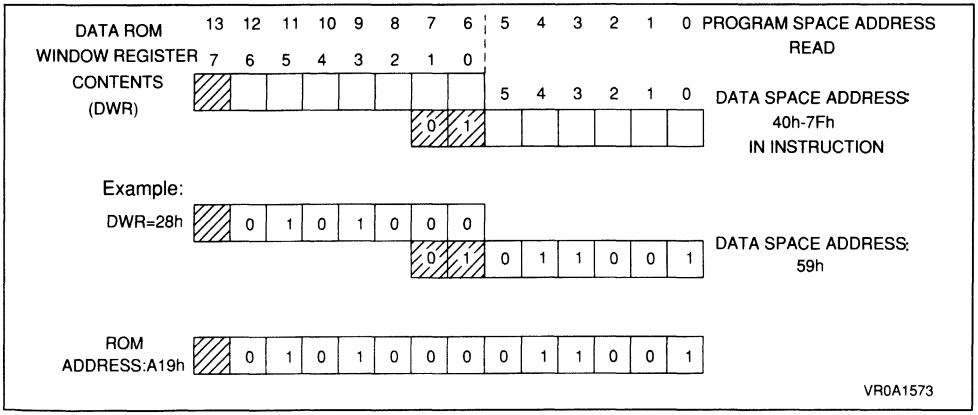
D7. This bit is not used.

DWR6-DWR0. These are the Data ROM Window bits that correspond to the upper bits of the data ROM space.

This register is undefined on reset. Neither read nor single bit instructions may be used to address this register.

Note: Care is required when handling the DWR register as it is write only. For this reason, it is not allowed to change the DWR contents while executing interrupt service routine, as the service routine cannot save and then restore its previous content. If it is impossible to avoid the writing of this register in the interrupt service routine, an image of this register must be saved in a RAM location, and each time the program writes to the DWR it must write also to the image register. The image register must be written first, so if an interrupt occurs between the two instructions the DWR is not affected.

Figure 9. Data ROM Window Memory Addressing



MEMORY SPACES (Continued)

Data RAM/EEPROM Bank Register (DRBR)

The selection of the bank is made by programming the Data RAM Bank Switch register (DRBR register) located at address E8h of the Data Space according to Table 2. No more than one bank should be set at a time.

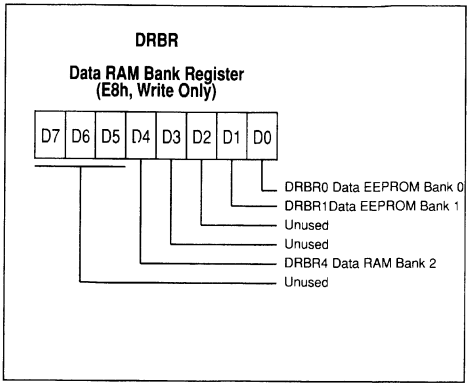
The DRBR register can be addressed like a RAM location in the Data Space at the address E8h; nevertheless it is a write only register that cannot be accessed with single-bit operations. This register is used to select the desired 64-byte RAM/EEPROM bank of the Data Space. The number of bank has to be loaded in the DRBR register and the instruction has to point to the selected location as if it was in bank 0 (from 00h address to 3Fh address).

This register is not cleared during the MCU initialization, therefore it must be written before the first access to the Data Space bank region. Refer to the Data Space description for additional information. The DRBR register is not modified when an interrupt or a subroutine occurs.

Table 2. Data RAM Bank Register Set-up

DRBR Value	Selection
00h	None
01h	EEPROM Page 0
02h	EEPROM Page 1
10h	RAM Page 2
Other	Reserved

Figure 11. Data RAM Bank Register



D7-D5. These bits are not used.

DRBR4. This bit, when set, selects RAM page 2.

D3-D2. These bits are not used.

DRBR1. This bit, when set, selects EEPROM page 1.

DRBR0. This bit, when set, selects EEPROM page 0.

Notes:

Care is required when handling the DRBR register as it is write only. For this reason, it is not allowed to change the DRBR contents while executing interrupt service routine, as the service routine cannot save and then restore its previous content. If it is impossible to avoid the writing of this register in interrupt service routine, an image of this register must be saved in a RAM location, and each time the program writes to DRBR it must write also to the image register. The image register must be written first, so if an interrupt occurs between the two instructions the DRBR is not affected.

In DRBR Register, *only 1 bit must be set.* Otherwise two or more pages are enabled in parallel, producing errors.

MEMORY SPACES (Continued)

EEPROM Description

The data space of ST62xx family from 00h to 3Fh is paged as described in Table 3. The ST6260/65 has 128 bytes of EEPROM located in two pages of 64 bytes (page 0 and 1).

The EEPROM is physically organized in 32 byte modules (2 modules per page) and does not require dedicated instructions to be accessed in reading or writing. Once selected through the Data RAM Bank Register, the active EEPROM page is controlled by the EEPROM Control Register (EECTL) located at address EAh. E20FF bit of the EECTL register must be cleared to "0" prior to any write or read access to the EEPROM. If no bank is selected or if E2OFF is set, any access is meaningless.

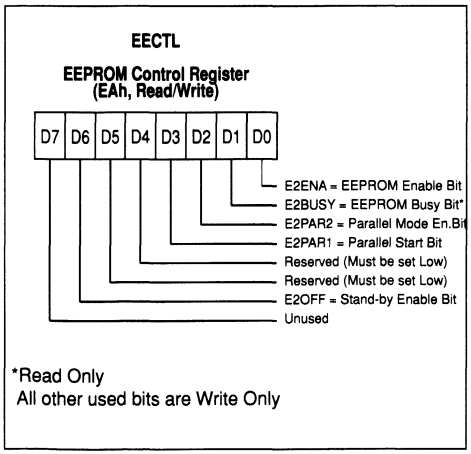
Programming must be enabled by setting bit E2ENA of register EECTL.

Bit E2BUSY of EECTL register is set to 1 when the EEPROM is performing a programming cycle. Any access to the EEPROM when E2BUSY is set to 1 is meaningless.

Provided E2OFF and E2BUSY are cleared to 0, an EEPROM location is read like any other data location, also in term of access time.

Writing the EEPROM can work in two modes: Byte Mode (BMODE) and Parallel Mode (PMODE). BMODE is the normal way to use the EEPROM and consists in accessing one byte at a time. PMODE consists in simultaneously programing 8 bytes of the same row.

Figure 12. EEPROM Control Register



*Read Only
All other used bits are Write Only

D7. Not Used

E2OFF. *WRITE ONLY.* If this bit is set the EEPROM is disabled (any access will be meaningless) and the power consumption of the EEPROM is reduced to the lowest values.

D5, D4. Reserved, must be set to zero.

E2PAR1. *WRITE ONLY.* Once in Parallel Mode, as soon as the user software sets the E2PAR1 bit the parallel writing of the 8 adjacent registers will start. It is internally reset at the end of the programming procedure. Note that less than 8 bytes can be written; the undefined bytes are unaffected by the parallel programming.

E2PAR2. *WRITE ONLY.* This bit must be set by the user program in order to perform parallel programming (more than one byte at a time). If E2PAR2 is set and the parallel start bit (E2PAR1) is low, up to 8 adjacent bytes can be written at maximum speed, the contents being stored in volatile registers. These 8 adjacent bytes are considered as a row, whose address lines A7, A6, A5, A4, A3 are fixed while A2, A1 and A0 are the changing bits. E2PAR2 is automatically reset at the end of any parallel programming procedure. It can be reset by the user software before starting the programming procedure, leaving the EEPROM registers unchanged.

E2BUSY. *READ ONLY.* This bit is automatically set by the EEPROM control logic when the EEPROM is in programming mode. The user program should test it before any read or write EEPROM operation; any attempt to access the EEPROM while the busy bit is set will be aborted and the writing procedure in progress completed.

E2ENA. *WRITE ONLY.* This bit enables programming of the EEPROM cells. It must be set to one before any write into the EEPROM register. Any attempt to write to the EEPROM when E2ENA is low is meaningless and will not trigger a write cycle.

This register is cleared at reset.

Notes:

The data to write has to be written directly at the address that it will have inside the EEPROM space. There is no buffer memory between the data RAM and the EEPROM spaces.

When the EEPROM is busy (E2BUSY = "1") EECTL can not be accessed in write mode, it is only possible to read the status of E2BUSY. This implies that as long as the EEPROM is busy, it is not possible to change the status of the EEPROM Control Register. EECTL bits 4 and 5 are reserved and must never be set to "1".

MEMORY SPACES (Continued)

Table 3. EEPROM Parallel Write Row Structure

Byte	0	1	2	3	4	5	6	7	Dataspace addresses. Banks 0 and 1.
ROW7									38h-3Fh
ROW6									30h-37h
ROW5									28h-2Fh
ROW4									20h-27h
ROW3									18h-1Fh
ROW2									10h-1Fh
ROW1									08h-0Fh
ROW0									00h-07h

Up to 8 bytes in each row may be programmed at the same time in Parallel Write mode

Additional Notes on Parallel Mode. If the user wishes to perform parallel programming, the first action should be to set the E2PAR2 bit to one. From this time the EEPROM will be addressed in writing, the ROW address will be latched and it will be possible to change it only at the end of the programming procedure or by resetting E2PAR2 without programming the EEPROM. After the ROW address latching the ST62xx can "see" only one EEPROM row (the selected one) and any attempt to write or read other rows will produce errors. Do not read the EEPROM while E2PAR2 is set.

As soon as E2PAR2 bit is set, the 8 volatile ROW latches are cleared. From this moment the user can load data in the whole ROW or in a subset. Setting E2PAR1 will modify the EEPROM registers corresponding to the ROW latches accessed after E2PAR2. For example, if the software sets E2PAR2 and accesses the EEPROM by writing to addresses 18h, 1Ah, 1Bh and then sets E2PAR1, these three registers will be modified at the same time; the remaining bytes will be unaffected. Note that E2PAR2 is internally reset at the end of the programming procedure. This implies that the user must set E2PAR2 bit between two parallel programming procedures. Note that if the user tries to set E2PAR1 while E2PAR2 is not set there will not be any programming procedure and the E2PAR1 bit will be unaffected. Consequently E2PAR1 bit cannot be set if E2ENA is low. E2PAR1 can be affected by the user to set it, only if E2ENA and E2PAR2 bits are also set to one.

TEST MODE

For normal operation the TEST pin must be held low when reset is active. An on-chip 100kΩ pull-down resistor is internally connected to the TEST pin.

INTERRUPTS

The ST62xx core can manage 4 different maskable interrupt sources, plus one non-maskable interrupt source (top priority level interrupt). Each source is associated with a particular interrupt vector that contains a Jump instruction to the related interrupt service routine. Each vector is located in the Program Space at a particular address (see Table 1). When a source provides an interrupt request, and the request processing is also enabled by the ST62xx core, then the PC register is loaded with the address of the interrupt vector (i.e. of the Jump instruction).
Finally, the PC is loaded with the address of the Jump instruction and the interrupt routine is processed.

The ST6260 and ST6265 microcontrollers have eight different interrupt sources associated to five interrupt vectors as it is described in table below.

Table 4. Interrupt Vector/Source Relationship

Interrupt Source	Vector	Vector Address
NMI	Interrupt vector #0	(FFCh, FFDh)
Port A & B	Interrupt vector #1	(FF6h, FF7h)
Port C & SPI	Interrupt vector #2	(FF4h, FF5h)
AR TIMER	Interrupt vector #3	(FF2h, FF3h)
TIMER1 & ADC	Interrupt vector #4	(FF0h, FF1h)

Interrupt Vectors Description

The ST62xx core includes 5 different interrupt vectors in order to branch to 5 different interrupt routines in the static page of the Program Space.

- The interrupt vector associated with the non-maskable interrupt source is named interrupt vector #0. It is located at addresses FFCh,FFDh in the Program Space. On ST6260 and ST6265 this vector is associated with the external falling edge sensitive interrupt pin (NMI).
- The interrupt vector located at addresses FF6h, FF7h is named interrupt vector #1. It is associated with Port A and Port B pins. It can be programmed by software either in the falling edge detection mode or in the low level sensitive detection mode according to the code loaded in the Interrupt Option Register (IOR).
- The interrupt vector located at addresses FF4h, FF5h is named interrupt vector #2. It is associate with Port C pins and the SPI peripheral can be programmed by software either in the falling edge detection mode or in the positive edge detection mode according to the code loaded in the Interrupt Option Register (IOR).
- The interrupt vector located at addresses FF2h, FF3h is named interrupt vector #3. It is associated with the AR TIMER peripheral.
- The interrrupt vector loaded at address FF0h, FF1h is named interrupt vector #4. It is associated with the TIMER 1 and the A/D converter peripherals.

All the on-chip peripherals have an interrupt request flag bit (TMZ for timer, EOC for A/D), this bit is set to one when the device wants to generate an interrupt request and a mask bit (ETI for timer, EAI for A/D) that must be set to one to allow the transfer of the flag bit to the core.

Interrupt Priority

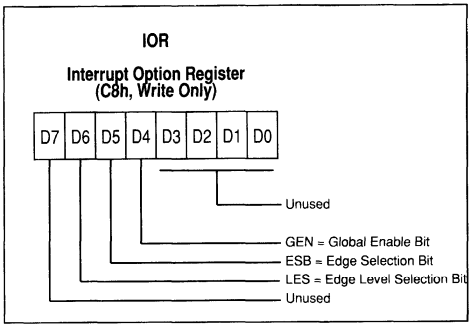
The non-maskable interrupt request NMI has the highest priority and can interrupt any other interrupt routines at any time, nevertheless the four other interrupts can not interrupt each other. If more than one interrupt request are pending, they are processed by the ST62xx core according to their priority level: vector #1 has the higher priority while vector #4 the lower.
The priority of each interrupt source is fixed.

INTERRUPT (Continued)

Interrupt Option Register

The Interrupt Option Register (IOR register, location C8h) is used to enable/disable the individual interrupt sources and to select the operating mode of the external interrupt inputs. This register can be addressed in the Data Space as RAM location at the address C8h, nevertheless it is a write-only register that cannot be accessed with single-bit operations. The operating modes of the external interrupt inputs associated to interrupt vectors #1 and #2 are selected through bits 5 and 6 of the IOR register.

Figure 13. Interrupt Option Register



D7. D3-D0 These bits are not used.

LES. Level/Edge Selection Bit. When this bit is set to one, the interrupt #1 (Port A, B lines) is low level sensitive, when cleared to zero the negative edge sensitive interrupt is selected.

ESB. Edge Selection Bit. When this bit is set to one, the interrupt #2 (Port C lines) is positive edge sensitive, when cleared to zero the negative edge sensitive interrupt is selected.

GEN. Global Enable Interrupt. When this bit is set to one, all the interrupts are enabled. When this bit is cleared to zero all the interrupts (excluding NMI) are disabled.

This register is cleared on reset.

Table 5. Interrupt Option Register Description

GEN	SET	Enable all interrupts
	CLEARED	Disable all interrupts
ESB	SET	Rising edge mode on interrupt input #2
	CLEARED	Falling edge mode on interrupt input #2
LES	SET	Level-sensitive mode on interrupt input #1
	CLEARED	Falling edge mode on interrupt input #1
OTHERS	NOT USED	

External Interrupts Operating Modes

The NMI interrupt is associated to the NMI pin of the ST6260/65. The interrupt request is generated by a falling edge applied to the NMI pin. The NMI interrupt pin signal is latched and is automatically reset by the core at the beginning of the non-maskable interrupt service routine. An on-chip pull-up resistor and a Schmitt trigger are available at pin NMI.

The two interrupt sources associated with the falling/rising edge mode of the external interrupt pins (Ports A and B vector #1, Ports C vector #2) are connected to two internal latches. Each latch is set when a falling/rising edge occurs and is cleared when the associated interrupt routine is started. So, the occurrence of an external interrupt request is stored: a second interrupt, that occurs during the processing of the first one, will be processed as soon as the first one has been finished (if there is not an higher priority interrupt request). If more than one interrupt occurs during the processing of the first one, these other interrupt requests will be lost.

The storage of the interrupt requests is not available in the level sensitive detection mode. To be taken into account, the low level must be present on the interrupt pin when the core samples the line after the execution of the instructions. At the end of each instruction the core tests the interrupt lines and if there is a pending interrupt request the next instruction is not executed and the related interrupt routine is executed.

Note:

When GEN bit is low, the NMI interrupt is active but cannot cause a wake up from STOP/WAIT modes.

INTERRUPT (Continued)

Interrupt Procedure. The interrupt procedure is very similar to a call procedure, indeed the user can consider the interrupt as an asynchronous call procedure. As this is an asynchronous event, the user does not know about the context and the time at which it occurred. As a result the user should save all the data space registers which will be used inside the interrupt routines. There are separate sets of processor flags for normal, interrupt and non-maskable interrupt modes which are automatically switched and so these do not need to be saved.

The following list summarizes the interrupt procedure:

ST62xx actions

- Interrupt detection
- The flags C and Z of the main routine are exchanged with the flags C and Z of the interrupt routine (or the NMI flags)
- The value of the PC is stored in the first level of the stack
- The normal interrupt lines are inhibited (NMI still active)
- First internal latch is cleared
- The related interrupt vector is loaded in the PC.

User actions

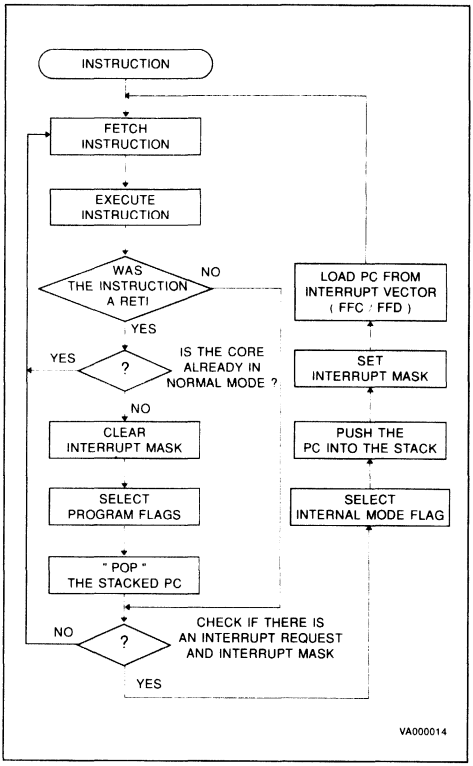
- User selected registers are saved inside the interrupt service routine (normally on a software stack)
- The source of the interrupt is found by polling (if more than one source is associated to the same vector) the interrupt flag of the source.
- Interrupt servicing
- Return from interrupt (RETI)

ST62xx actions

- Automatically the ST62xx core switches back to the normal flags (or the interrupt flags) and pops the previous PC value from the stack

The interrupt routine begins usually by the identification of the device that has generated the interrupt request (by polling). The user should save the registers which are used inside the interrupt routine (that holds relevant data) into a software stack. After the RETI instruction execution, the core carries out the previous actions and the main routine can continue.

Figure 14. Interrupt Processing Flow-Chart



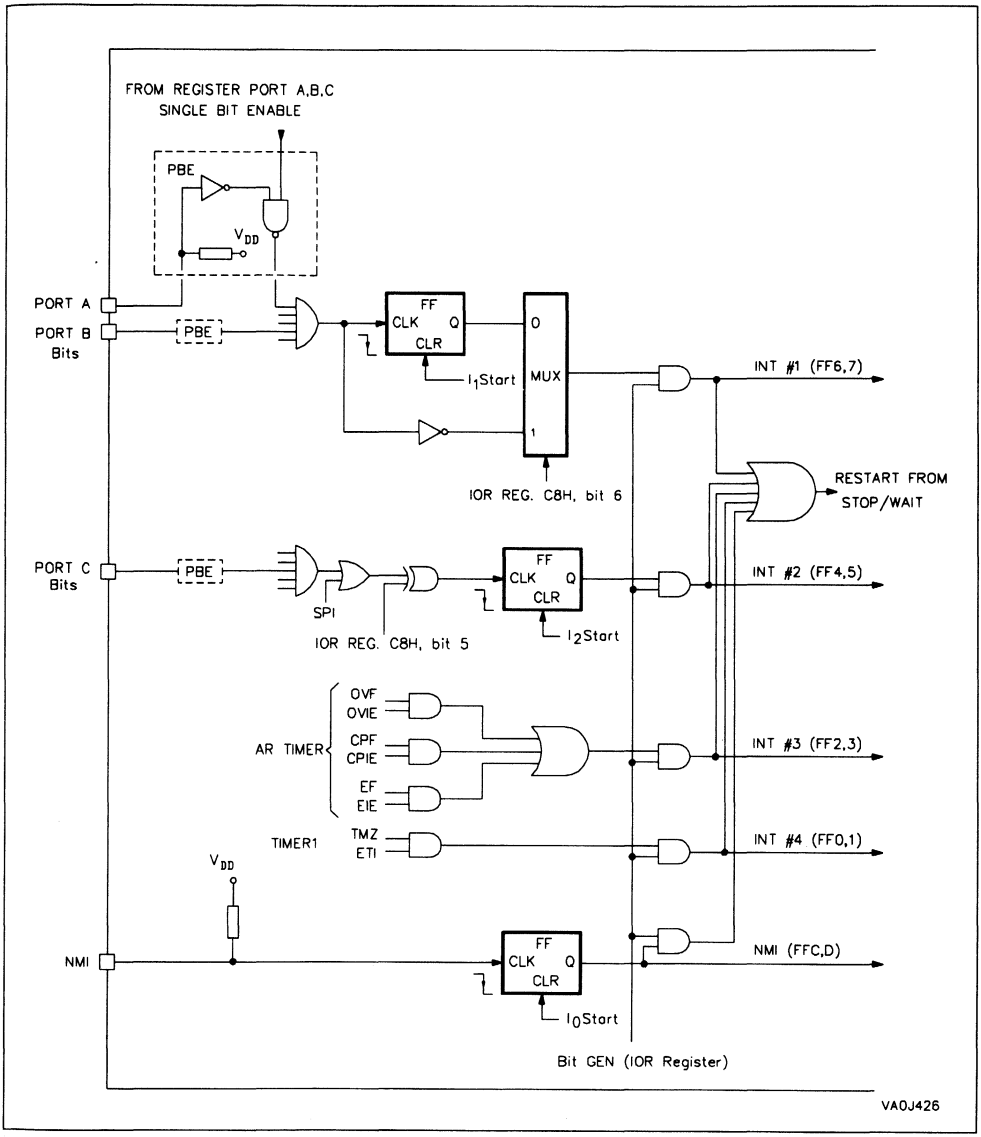
INTERRUPT (Continued)

Table 6. Interrupt Requests and Mask Bits

Peripheral	Register	Register Address	Mask bit	Masked Interrupt Source
All	IOR	C8h	GEN	All Interrupts, excluding NMI
I/O Ports	IOR	C8h	GEN	All I/O Pins Interrupt Request
TIMER 1	TSCR1	D4h	ETI	TMZ: TIMER 1 Overflow
A/D Converter	ADCR	D1h	EAI	EOC: End of Conversion
AR TIMER	ARMC	D5h	OVIE CPIE EIE	OVF: AR TIMER Overflow CPF: Successful compare EF: Active edge on ARTIMin
SPI	SPIMOD	E2h	SPIE	SPIF: End of Transmission

INTERRUPT (Continued)

Figure 15. Interrupt Circuit Diagram



RESET

The ST6260/65 can be reset in three ways: by the external reset input ($\overline{\text{RESET}}$) tied low, by power-on reset and by the digital Watchdog peripheral

RESET Input

The $\overline{\text{RESET}}$ pin can be connected to a device of the application board in order to restart the MCU during its operation. The activation of the $\overline{\text{RESET}}$ pin may occur in the RUN, WAIT or STOP mode. This input has to be used to reset the MCU internal state and provide a correct start-up procedure. The pin is active low and has a schmitt trigger input. The internal reset signal is generated by adding a delay to the external signal. Therefore even short pulses at the $\overline{\text{RESET}}$ are accepted, provided V_{DD} has finished its rising phase and the oscillator is running correctly (normal RUN or WAIT modes). The MCU is kept in the Reset state as long as the $\overline{\text{RESET}}$ pin is held low.

If the $\overline{\text{RESET}}$ activation occurs in the RUN or WAIT mode, the processing of the program is stopped (in RUN mode only) and the Input/Outputs are placed in input with pull-up resistors. When the level on the $\overline{\text{RESET}}$ pin becomes high, the initialization sequence is executed just after the internal delay.

If a $\overline{\text{RESET}}$ pin activation occurs in the STOP mode, the oscillator starts and all the inputs/outputs are configured in input with pull-up resistors. When the level of the $\overline{\text{RESET}}$ pin becomes high, the initialization sequence is started just after the internal delay.

Power-on Reset

The function of the POR consists in waking up the MCU during the power-on sequence. At the beginning of this sequence, the MCU is configured in the Reset state: every Input/Output port is configured in input with pull-up resistor and no instruction is executed. When the power supply voltage becomes sufficient, the oscillator starts to operate, nevertheless an internal delay is generated to allow the oscillator to be completely stabilized before the execution of the first instruction. The initialization sequence is executed just after the internal delay.

The internal delay is generated by an on-chip counter. This releases the internal reset of the MCU 2048 oscillator cycles after the $\overline{\text{RESET}}$ pin becomes high.

Note:

To have a correct start-up, the user should take care that the internal reset is not released before the V_{DD} level is sufficient to allow MCU operation at the chosen frequency (see Recommended Operating Conditions).

A proper reset signal for slow rising V_{DD} can be generally provided by an external RC network connected at pin $\overline{\text{RESET}}$.

RESET (Continued)

Watchdog Reset

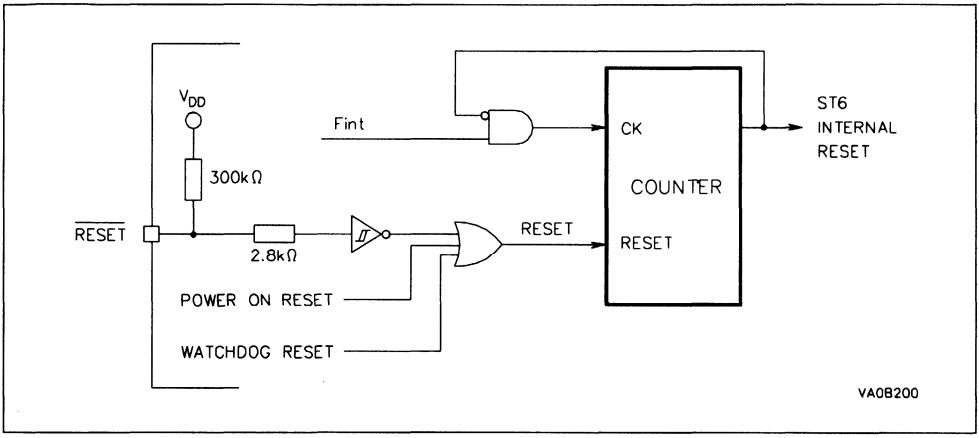
The ST6260 and ST6265 provide an on-chip watchdog function in order to provide a graceful recovery from a software upset. If the watchdog register is not refreshed, preventing the end-of-count being reached, the internal reset is activated. This, in particular, resets the watchdog. The MCU restarts as with normal reset from $\overline{\text{RESET}}$ pin including the internal delay.

Application Notes

An external resistor between V_{DD} and reset pin is not required because an internal pull-up device is provided.

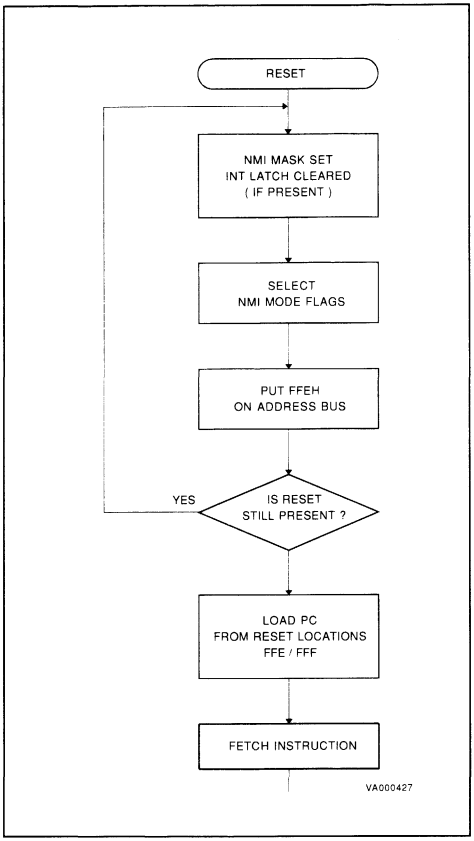
The POR device operates in a dynamic manner in the way that it brings about the initialization of the MCU when it detects a dynamic rising edge of the V_{DD} voltage. The typical detected threshold is about 2 volts, but the actual value of the detected threshold depends on the way in which the V_{DD} voltage rises up. The POR device *DOES NOT* allow the supervision of a static or slowly rising or falling edge of the V_{DD} voltage.

Figure 16. Reset Circuit



RESET (Continued)

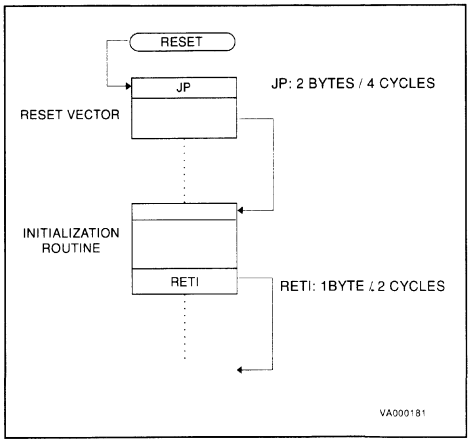
Figure 17. Reset and Interrupt Processing Flow-Chart



MCU Initialization Sequence

When a reset occurs the stack is reset to the program counter, the PC is loaded with the address of the reset vector (located in the program ROM at addresses FFEh & FFFh). A jump instruction to the beginning of the program has to be written into these locations. After a reset a NMI is automatically activated so that the core is in non-maskable interrupt mode to prevent false or ghost interrupts during the restart phase. Therefore the restart routine should be terminated by a RETI instruction to switch to normal mode and enable interrupts. If no pending interrupt is present at the end of the reset routine the ST62xx will continue with the instruction after the RETI; otherwise the pending interrupt will be serviced

Figure 18. Restart Initialization Program Flow-Chart



RESET (Continued)

Table 7. Reset Value

Register	Address	Value	Comment
Oscillator Control Register	0DCh		$f_{INT} = f_{OSC}$; user must set bit3 to 1
Data RAM Page Register	0E8h		All Data Banks disabled
EEPROM Control Register	0EAh		EEPROM disabled
Port Data Registers	0C0h to 0C3h		
Port Direction Register	0C4h to 0C6h		I/O are Input with pull-up
Port Option Register	0CCh to 0CEh		I/O are Input with pull-up
Interrupt Option Register	0C8h		Interrupt disabled
Data ROM Window Register	0C9h		Timer 1 disabled
Timer 1 Status/Control	0D4h	00h	
			AR Timer stopped
AR Timer Mode Control Register	005h		
AR Timer Status/Control 1 Register	006h		
AR Timer Status/Control 2 Register	007h		
AR Timer Compare Register	0DAh		
Miscellaneous Register	0DDh		SPI output not connected to PC3
SPI Registers	0E0h to 0E2h		SPI disabled
X, Y, V, W, Register	080h to 083h		
Accumulator	0FFh		
Data RAM	084h to 0BFh		
EEPROM	00h to 03Fh	Undefined	
A/D Result Register	0D0h		
AR Timer Load Register	0DBh		
AR Timer Reload/Capture Register	0D9h		
Timer 1 Counter Register	0D3h	FFh	
Timer 1 Prescaler Register	0D2h	7Fh	Max count loaded
Watchdog Counter Register	0D8h	FEh	Software Watchdog (1)
		FFh	Hardware Watchdog (1)
A/D Control Register	0D1h	40h	A/D in Standby

Note 1. Mask option selected

WAIT & STOP MODES

The WAIT and STOP modes have been implemented in the ST62xx core in order to reduce the consumption of the product when the latter has no instruction to execute. These two modes are described in the following paragraphs

WAIT Mode

The MCU goes into the WAIT mode as soon as the WAIT instruction is executed. The microcontroller can also be considered as being in a "software frozen" state where the core stops processing the instructions of the routine, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage, but where the peripherals are still working.

The WAIT mode can be used when the user wants to reduce the consumption of the MCU when it is idle, while not losing count of time or monitoring of external events. The oscillator is not stopped in order to provide a clock signal to the peripherals. The Timer 1 and auto-reload Timer counting may be enabled as well as both Timer interrupts before entering the WAIT mode; this allows the WAIT mode to be left when timer interrupt occurs. The above explanation related to the timers applies also to the A/D converter and the SPI.

If the exit from the WAIT mode is performed with a general RESET (either from the activation of the external pin or by watchdog reset) the MCU enters a normal reset procedure as described in the RESET chapter. If an interrupt is generated during WAIT mode the MCU behavior depends on the state of the ST62xx core before the initialization of the WAIT sequence, but also of the kind of the interrupt request that is generated. This case is described in the following paragraphs. In any case, the ST62xx core does not generate any delay after the occurrence of the interrupt because the oscillator clock is still available.

STOP Mode

If the Watchdog is disabled the STOP mode is available. When in STOP mode the MCU is placed in the lowest power consumption mode. In this operating mode the microcontroller can be considered as being "frozen", no instruction is executed, the oscillator is stopped, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage, and the ST62xx core waits for the occurrence of an external interrupt request or Reset activation to output from the STOP state.

If the exit from the STOP mode is performed with a general RESET (by the activation of the external pin) the MCU will enter a normal reset procedure as described in the RESET chapter. The case of an interrupt depends on the state of the ST62xx core before the initialization of the STOP sequence and also of the kind of the interrupt request that is generated.

This case will be described in the following paragraphs. In any case, the ST62xx core generates a delay after the occurrence of the interrupt request in order to wait the complete stabilization of the oscillator before the execution of the first instruction.

Exit from WAIT and STOP Modes

The following paragraphs describe the output procedure of the ST62xx core from WAIT and STOP modes when an interrupt occurs (not a RESET). It must be noted that the restart sequence depends on the original state of the MCU (normal, interrupt or non-maskable interrupt mode) before the start of the WAIT or STOP sequence, but also of the type of the interrupt request that is generated.

Normal Mode. If the ST62xx core was in the main routine when the WAIT or STOP instruction has been executed, the ST62xx core outputs from the stop or wait mode as soon as any interrupt occurs; the related interrupt routine is executed and at the end of the interrupt service routine the instruction that follows the STOP or the WAIT instruction is executed if no other interrupts are pending.

WAIT & STOP MODES (Continued)

Not Maskable Interrupt Mode. If the STOP or WAIT instruction has been executed during the execution of the non-maskable interrupt routine, the ST62xx core outputs from the stop or wait mode as soon as any interrupt occurs: the instruction that follows the STOP or the WAIT instruction is executed and the ST62xx core is still in the non-maskable interrupt mode even if another interrupt has been generated.

Normal Interrupt Mode. If the ST62xx core was in the interrupt mode before the initialization of the STOP or WAIT sequence, it outputs from the stop or wait mode as soon as any interrupt occurs. Nevertheless, two cases have to be considered:

- If the interrupt is a normal interrupt, the interrupt routine in which the wait or stop was entered will be completed with the execution of the instruction that follows the STOP or the WAIT and the ST6xx core is still in the interrupt mode. At the end of this routine pending interrupts will be serviced in accordance to their priority.
- If the interrupt is a non-maskable interrupt, the non-maskable routine is processed at first. Then the routine in which the wait or stop was entered will be completed with the execution of the instruction that follows the STOP or the WAIT and the ST6xx core remains in the normal interrupt mode.

Notes:

To reach the lowest power consumption during RUN or WAIT modes, the user software must take care of:

- selecting 4 as ratio of the Oscillator divider.
- configuring unused I/O as input without pull-up with well defined logic levels.
- placing the A/D converter in its power down mode by clearing the PDS bit in the A/D control register before entering the STOP instruction.
- putting the EEPROM on-chip memory in standby mode by setting the E2OFF bit in EEPROM Control Register to one.

When the hardware activated watchdog is selected or the software watchdog enabled, the STOP instruction is deactivated and any attempt to execute the STOP instruction will cause an execution of a WAIT instruction.

If all the interrupt sources are disabled (including NMI if GEN is low), the restart of the MCU can only be done by a Reset activation. The WAIT and STOP instructions are not executed if an enabled interrupt request is pending.

ON-CHIP CLOCK OSCILLATOR

The ST6260/65 on-chip oscillator has been designed to require a minimum of external components and to reduce the oscillator power consumption.

A quartz crystal, a ceramic resonator or an external signal (provided to the OSCin pin) may be used to generate a system clock with various stability/cost tradeoffs. The clock generator options connection methods are shown in Figure 21.

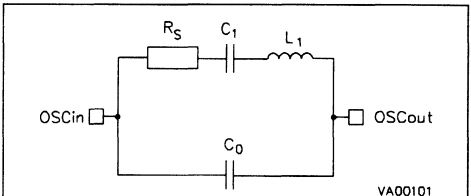
A programmable divider is provided in order to adjust the internal clock of the micro (core and peripherals) to the best power consumption/performance trade-off. The Division Ratio is selected through the Oscillator Control Register located at address 0DCh.

The internal frequency is directly used to clock the A/D Converter and the AR Timer. It is further divided by 12 to produce the Timer 1 and Watchdog clock and by 13 for the core and SPI clock.

With a 8MHz external frequency, the fastest machine cycle is therefore 1.625µs.

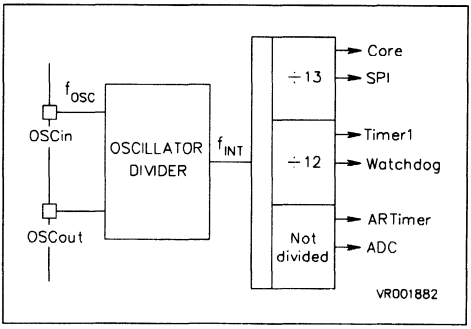
The machine cycle is the smallest unit needed to execute any operation (i.e.increment the program counter). An instruction may need two, four, or five machine cycles to be executed.

Figure 20. Crystal Parameters



Crystal Parameters: AT-cut Parallel Resonance Crystal
C0 = Parallel Resonance Capacitance

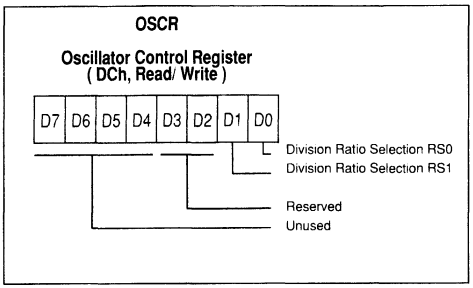
Figure 19. Internal Clock Circuits



ON-CHIP CLOCK OSCILLATOR (Continued)

Oscillator Control Register

Figure 21. Oscillator Control Registers



D7-D4. These bits are not used.

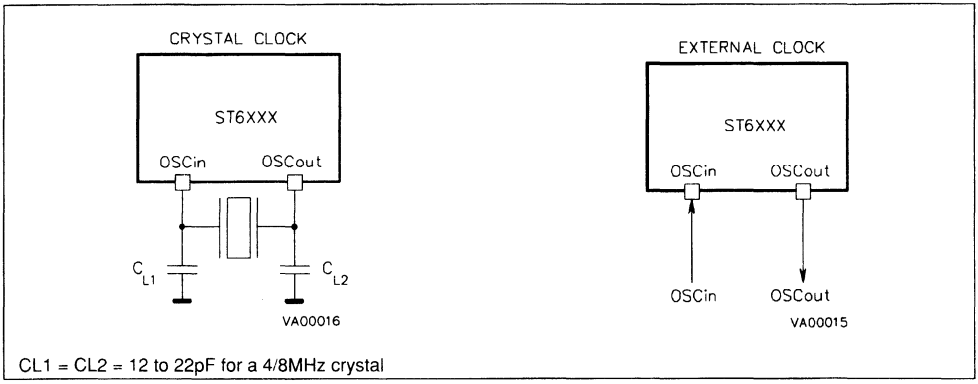
D3. Reserved - Cleared at Reset. THIS BIT MUST BE SET TO 1 BY USER PROGRAM to achieve lowest power consumption.

D2. Reserved must be kept low.

RS1-RS0. These bits select the division ratio of the Oscillator Divider in order to generate the internal frequency. The following selections are available:

RS1	RS0	Division Ratio
0	0	1
0	1	2
1	0	4
1	1	4

Figure 22. Oscillator Connection



CL1 = CL2 = 12 to 22pF for a 4/8MHz crystal

INPUT/OUTPUT PORTS

The ST6260 and ST6265 microcontroller have respectively 13 and 21 Input/Output lines that can be individually programmed either in the input mode or the output mode with the following software selectable options:

- Input without pull-up and without interrupt
- Input with pull-up and with interrupt
- Input with pull-up without interrupt
- Analog inputs (PA0-PA7, PC0-PC3)
- Timer 1 I/O line (PC1, not available on ST6260)
- AR Timer I/O lines (PB6, PB7)
- SPI control signals (PC2-PC4)
- Push-pull output
- Standard Open drain output
- 20mA Open drain output PB lines.

The lines are organized in three Ports (Port A, B and C).

Each port occupies 3 registers in the data space. Each bit of these registers is associated with a particular line (for instance, the bits 0 of the Port A Data, Direction and Option registers are associated with the PA0 line of Port A).

The three DATA registers (DRA, DRB, DRC), are used to read the voltage level values of the lines programmed in the input mode, or to write the logic value of the signal to be output on the lines configured in the output mode. The port data registers can be read to get the effective logic levels of the pins, but they can be also written by the user software, in conjunction with the related option registers, to select the different input mode options.

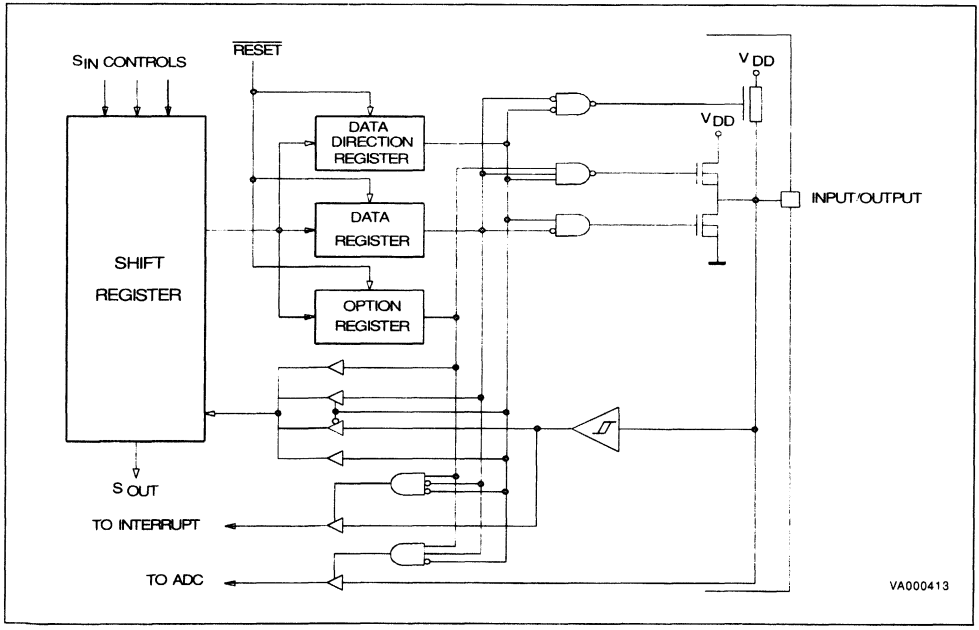
Single-bit operations on I/O registers are possible but care is necessary because reading in input mode is done from I/O pins while writing will directly affect the Port data register causing an undesired change of the input configuration.

The three Data Direction registers (DDRA, DDRB and DDRC) allow the selection of the data direction of each pin (input or output).

The three Option registers (ORPA, ORPB and ORPC) are used to select the different port options available both in input and in output mode.

All the I/O registers can be read or written as any other RAM location of the data space, so no extra RAM cell is needed for port data storing and manipulation. During the initialization of the MCU, all the I/O registers are cleared and the input mode with pull-up/no-interrupt is selected on all the pins, thus avoiding pin conflicts.

Figure 23. I/O Port Block Diagram



INPUT/OUTPUT PORTS (Continued)

I/O Pin Programming

Each pin can be individually programmed as input or output with different input and output configurations.

This is achieved by writing the relevant bit in the data (DR), data direction register (DDR) and option registers (OR). Table 7 shows all the port configurations that can be selected by user software.

Input Option Description

Pull-up, High Impedance Option. All the input lines can be individually programmed with or without an internal pull-up according to the codes programmed in the OR and DR registers . If the pull-up option is not selected, the input pin is in the high-impedance state.

Interrupt Option. All the input lines can be individually connected by software to the interrupt lines of the ST62xx core according to the codes programmed in the OR and DR registers. The pins of Port A and B are "ORed" and are connected to the interrupt associated to the vector #1. Pins of ports C are "ORed" with the SPI interrupt line and connected to interrupt vector #2. The interrupt modes (falling edge sensitive, rising edge sensitive) can be selected by software for each port by programming the IOR register.

Analog Input Option. The seven PA5-PA7, PB0-PB3 pins can be configured to be analog inputs according to the codes programmed in the OR and DR registers. These analog inputs are connected to the on-chip 8-bit Analog to Digital Converter. *ONLY ONE* pin should be programmed as analog input at a time, otherwise the selected inputs will be shorted.

Figure 24. I/O Port Data Registers

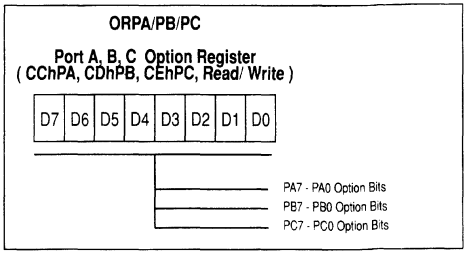


Figure 25. I/O Port Data Direction Registers

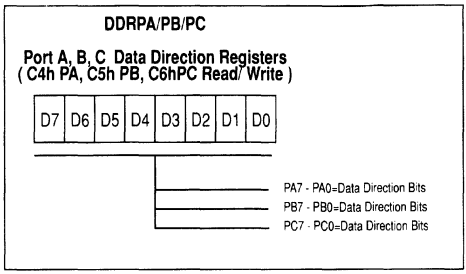
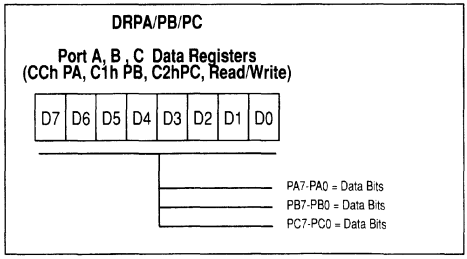


Figure 26. I/O Port Option Registers



Note: For complete coding explanation refer to Table 7

I/O Port Options Selection

DDR	OR	DR	Mode	Option
0	0	0	Input	With pull-up, no interrupt (Reset state)
0	0	1	Input	No pull-up, no interrupt
0	1	0	Input	With pull-up, with interrupt
0	1	1	Input	No pull-up, no interrupt (Port B pins)
			Input	Analog input (Ports A and C pins)
1	0	X	Output	Open-drain output (20mA sink current for Port B pins)
1	1	X	Output	Push-pull output (20mA sink current for Port B pins)

Notes: X. Means don't care.

INPUT/OUTPUT PORTS (Continued)

Timer 1 Alternate function Option.

When bit TOUT of register TSCR1 is low, pin PC1/Timer 1 is configured through the port registers as any standard pin of Port B. It is in addition connected to the Timer 1 input for Gated and Event counter modes. When bit TOUT of register TSCR1 is high, pin PC1/Timer 1 is forced as Timer 1 output. The port registers configuration is meaningless.

AR Timer Alternate function Option

When bit PWMOE of register ARMC is low, pin ARTIMout/PB7 is configured as any standard pin of port B through the port registers. When PWMOE is high, ARTIMout/PB7 is the PWM output. The port registers configuration is meaningless.

ARTIMin/PB6 is connected to the AR Timer input. It is configured through the port registers as any standard pin of port B. To use ARTIMin/PB6 as AR Timer input, it must be configured as input through DDRB.

PC2/PC4 are used as standard I/O as long as SPCLK is kept low.

PC3/SOUT is configured as SPI push-pull output by setting bit 0 of the Miscellaneous register (address 0DDh), regardless of the state of Port C registers.

PC4/SCK is configured as push-pull output clock (master mode) by programming it as push-pull output through DDRC register and by setting bit SPCLK of the SPI Mode Register.

PC4/SCK is configured as input clock (slave mode) by programming it as input through DDRC register and by clearing bit SPCLK of the SPI Mode Register. With this configuration, PC4 can simultaneously be used as an input.

Note. Switching the I/O ports from one state to another should be done in a way that no unwanted side effects can happen. The recommended safe transitions are shown below. All other transitions are risky and should be avoided during change of operation mode as it is most likely that there will be an unwanted side-effect such as interrupt generation or two pins shorted together by the analog input lines.

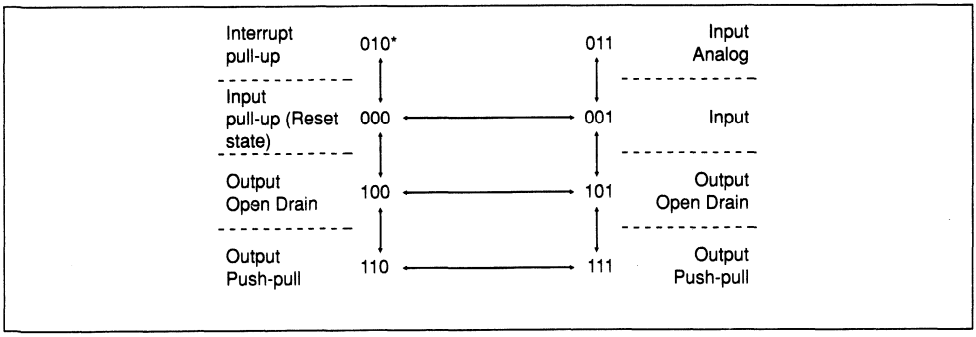
Single bit SET and RES instructions should be used very carefully with Port A and B data registers because these instructions make an implicit read and write back of the whole addressed register byte. In port input mode however data register address reads from input pins, not from data register latches and data register information in input mode is used to set characteristics of the input pin (interrupt, pull-up, analog input), therefore these characteristics may be unintentionally reprogrammed depending on the state of input pins. As general rule is better to use SET and RES instructions on data register only when the whole port is in output mode. If input or mixed configuration is needed it is recommended to keep a copy of the data register in RAM. On this copy it is possible to use single bit instructions, then the copy register could be written into the port data register.

```
SET     bit, datacopy
LD      a, datacopy
LD      DRA, a
```

The WAIT and STOP instructions allow the ST62xx to be used in situations where low power consumption is needed. The lowest power consumption is achieved by configuring I/Os in input mode with well-defined logic levels.

The user has to take care not to switch outputs with heavy loads during the conversion of one of the analog inputs in order to avoid any disturbance in the measurement.

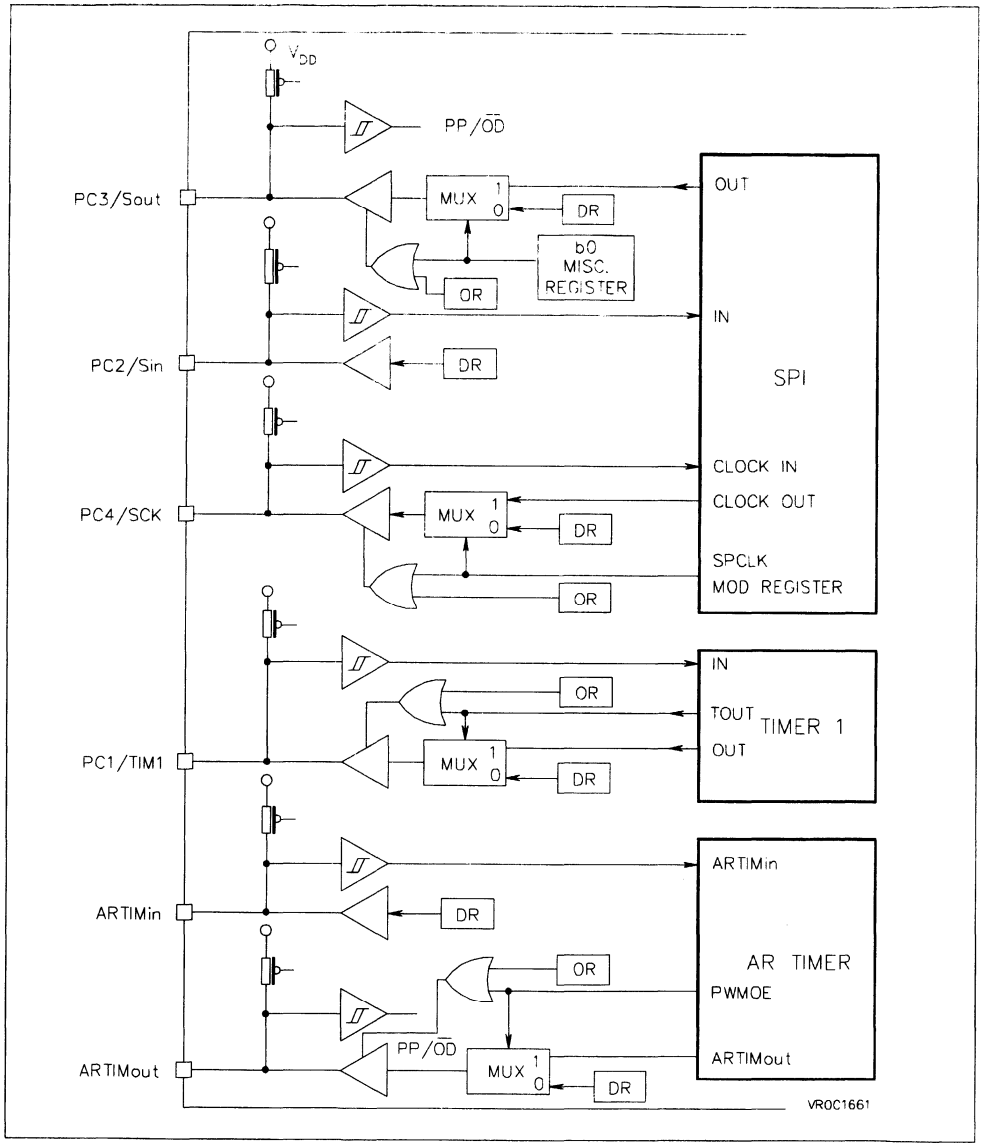
State Transition Diagram for Safe Transitions



Note *. xxx = DDR, OR, DR Bits respectively

INPUT/OUTPUT PORTS (Continued)

Figure 27. Peripheral Interface Configuration of SPI, Timer 1 and AR Timer



TIMERS

The ST6260/65 offer two on-chip Timer peripherals named Timer 1 and Auto-reload Timer. Timer 1 consists of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and control logic that allows configuring the peripheral in three operating modes. The Auto-reload Timer is an 8-bit Timer with Auto-reload, Input Capture and Output Compare capabilities. 4 modes are available for PWM, PLL, time measurement and period measurement.

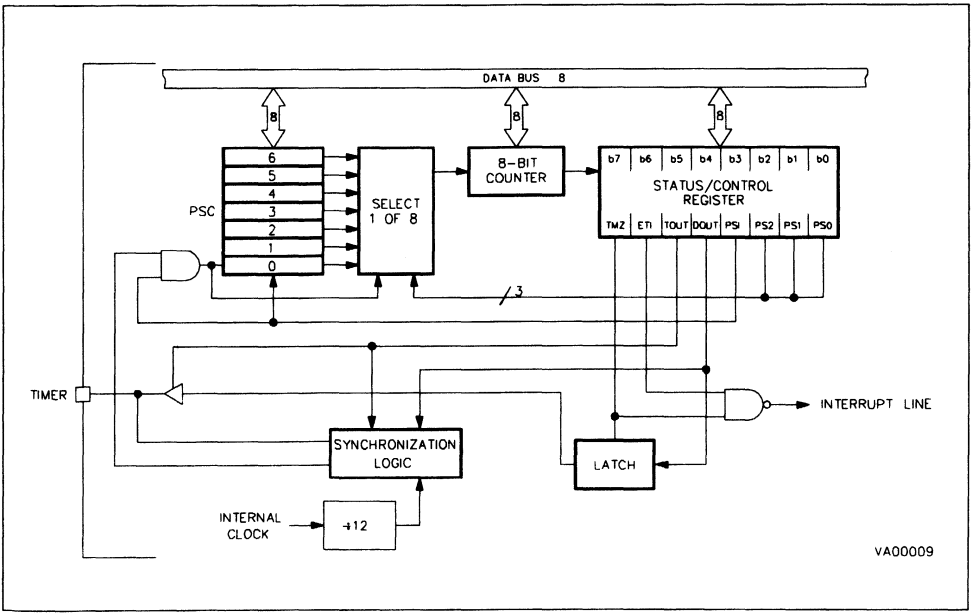
Timer 1

Figure 28 shows the Timer 1 block diagram. An external Timer pin is available for the user (ST6265 only). The content of the 8-bit counter can be read/written in the Timer/Counter register TCR which is addressed in the data space as a RAM location at addresses D3h. The state of the 7-bit prescaler is read in the PSC register at addresses D2h. The control logic device is managed in the TSCR1 register (addresses D4h) as described in the following paragraphs.

The 8-bit counter is decremented by the output (rising edge) coming from the 7-bit prescaler and can be loaded and read under program control. When it decrements to zero then the TMZ (Timer Zero) bit in the TSCR1 is set to one. If the ETI (Enable Timer Interrupt) bit in the TSCR1 is also set to one an interrupt request, associated to interrupt vector #4, is generated. The interrupt service routine then should poll bit TMZ in TSCR1 to determine if the interrupt has been generated by Timer 1 or by the A/D Converter. The Timer 1 interrupt can be used to exit the MCU from the WAIT mode.

The Timer 1 Prescaler input can be the internal clock (after Oscillator Divider) divided by 12 or an external clock at the Timer I/O pin. The prescaler decrements on the rising edge. Depending on the division factor programmed by PS2, PS1 and PS0 bits in TSCR1, the clock input of the timer/counter register is multiplexed to different sources. On division factor 1, the clock input of the prescaler is also that of timer/counter; on factor 2, bit 0 of prescaler register is connected to the clock input of TCR1. This bit changes its state with the half frequency of prescaler clock input. On factor 4, bit 1 of PSC1 is connected to clock input of TCR1, and so on. The prescaler initialize bit PSI in the TSCR1 register must be set to one to allow the prescaler (and hence the counter) to start. If it is cleared to zero then

Figure 28. Timer 1 Peripheral Block Diagram



TIMERS (Continued)

all of the prescaler bits are set to one and the counter is inhibited from counting. The prescaler can be given any value between 0 and 7Fh by writing to addresses D2h, if bit PSI in the TSCR1 register is set to one. The tap of the prescaler is selected using the PS2,PS1,PS0 bits in the control register. Figure 29 shows the Timer 1 working principle.

Timer 1 can be configured in 3 modes using the TOUT and DOUT bits of the TSCR1 register. These modes are Event counter, Gated or Output signal.

The internal Timer I/O can in addition be connected to either the PC1/TIM1 pin or the DRC1 bit depending on the configuration of bit DDRC1. Table 8 summarize the modes of Timer 1.

- Event counter: The Prescaler is decremented at each rising edge of the Timer I/O. The Timer I/O is either the PC1/TIM1 pin or the DRC1 bit of the DRC register depending on DDRC1.
- Gated: The Timer 1 is decremented by the Timer clock (f_{INT} divided by 12) when the internal Timer I/O is held high. The Timer I/O is either pin PC1/TIM1 or the DRC1 bit of register DDRC1.

Output signal: The PC1/TIM1 pin is connected to the DOUT latch and is configured as output regardless of DOUT and DDRC1 bits. The low to high transition of bit TMZ (when counter reaches 00h) is used to latch the data previously stored in DOUT and pass it to the PC1/TIM1 through the Timer I/O. This operating mode allows signal generation.

Timer 1 Interrupt

When the counter register decrements to zero and the software controlled ETI (Enable Timer Interrupt) bit is set to one then an interrupt request associated to interrupt vector #4 is generated. When the counter decrements to zero also the TMZ bit in the TSCR register is set to one.

Since only one interrupt vector is available for both Timer 1 and the A/D Converter, the interrupt service routine should determine from which source the interrupt came by polling the TMZ bit and the EOC bit of the A/D Converter Control Register.

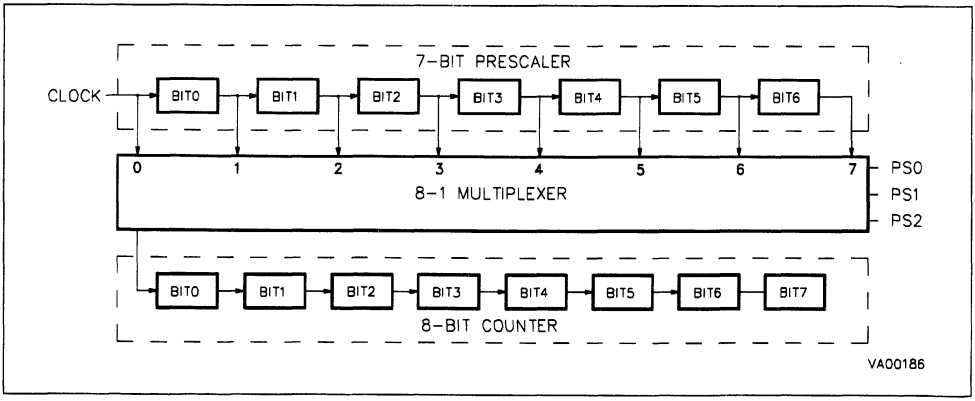
Notes:

TMZ is set when the counter reaches 00h; however, it may be set by writing 00h in the TCR1 register or setting bit 7 of the TSCR1 register. TMZ bit must be cleared by user software when servicing the Timer 1 interrupt to avoid undesired interrupts when leaving the interrupt service routine. After reset, the 8-bit counter register is loaded to FFh while the 7-bit prescaler is loaded to 7Fh , and the TSCR1 register is cleared which means that Timer 1 is stopped and the Timer 1 interrupt is disabled.

If the Timer 1 is programmed in output mode, DOUT bit is transferred to the TIM1 pin when TMZ is set to one (by software or due to counter decrement). When TMZ is high, the latch is transparent and DOUT is copied to the timer pin. When TMZ goes low, DOUT is latched.

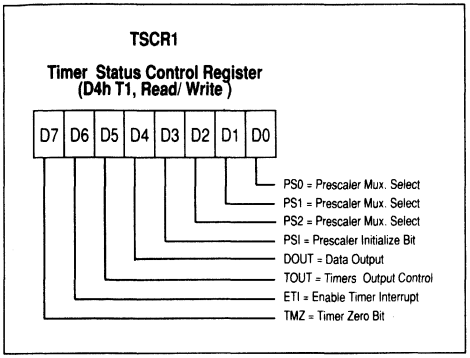
A write to the TCR1 register will predominate over the 8-bit counter decrement to 00h function, i.e. if a write and a TCR1 register decrement to 00h occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter reaches 00h again. The values of the TCR1 and the PSC1 registers can be read accurately at any time.

Figure 29. Timer1 Working Principle



TIMERS (Continued)

Figure 30. Timer Status Control Register



TMZ. Low-to-high transition indicates that the timer count register has decremented to zero. This bit must be cleared by user software before starting with a new count.

ETI. This bit, when set, enables the timer interrupt request (vector #4). If ETI="0" the timer interrupt is disabled. If ETI="1" and TMZ="1" an interrupt request is generated.

TOUT. When low, this bit selects an input mode for the Timer I/O pin. When high the output mode is selected.

DOUT. If Timer 1 is in Output mode, DOUT is the data sent to the PC1/TIM1 pin when TMZ goes high. DOUT enables discrimination between Event Counter and Gated modes if TOUT is low.

PSI. Used to initialize the prescaler and inhibit its counting. When PSI="0" the prescaler is set to 7Fh and the counter is inhibited. When PSI="1" the prescaler is enabled to count downwards. As long as PSI="0" both counter and prescaler are not running.

PS2, PS1, PS0. These bits select the division ratio of the prescaler register.

Table 8. Prescaler Division Factors

PS2	PS1	PS0	Divided by	PS2	PS1	PS0	Divided by
0	0	0	1	1	0	0	16
0	0	1	2	1	0	1	32
0	1	0	4	1	1	0	64

Figure 31. Timer Counter Register

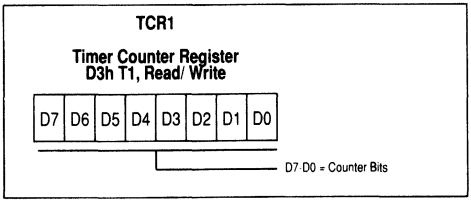


Figure 32. Prescaler Register

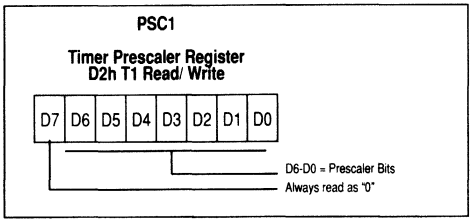


Table 9. Modes of Timer 1

TOUT	DOUT	DDRC1	Mode	Timer I/O
0	0	0	Event Counter	PC1/TIM1
0	0	1	Event Counter	DRC1
0	1	0	Gated	PC1/TIM1
0	1	1	Gated	DRC1
1	X	X	Output	PC1/TIM1

TIMERS (Continued)

Auto-reload Timer

The Auto-reload Timer (AR Timer) on-chip peripheral consists of an 8-bit timer/counter (AR COUNTER) with compare and capture/reload capabilities and a 7-bit prescaler with a clock multiplexer enabling the clock input to be selected as f_{INT}, $f_{INT}/3$ or external clock. One Mode Control Register (AR MODE), two Status Registers (ARSC0, ARSC1), an output pin (ARTIMout/PB7) and an input pin (ARTIMin/PB6) allow the Auto-reload Timer to be used in 4 modes:

- Auto-reload (PWM generation),
- Output compare and reload on external event (PLL),
- Input capture and output compare for time measurement.
- Input capture and output compare for period measurement.

The AR Timer can be used to wake the MCU from WAIT mode with either an internal or an external clock. It also can be used to wake the MCU from STOP mode if used with an external clock provided at pin ARTIMin. A Load register allows the program to read and write the counter on the fly.

AR Timer Description

The AR COUNTER is an 8-bit up-counter incremented on the clock input rising edge. It is loaded from the ReLoad/Capture Register REL/CAP (address D9h) for auto-reload or capture operations as well as for initialization. Direct access to the AR COUNTER is not possible, however by reading/writing the Load Register AR LOAD (address DBh) it is possible to read/write the TC counter content.

The AR Timer input clock is either the internal clock (from Oscillator Divider), the internal clock divided by 3 or the ARTIMin pin. Selection between these clock sources is made through the AR Multiplexer by bits CC0-CC1 of Register ARSCR1. The output of the AR Multiplexer feeds the AR Prescaler, ARPSC. ARPSC is a software programmable 7 bit prescaler. Programming of ARPSC is performed by the AR Prescaler Multiplexer AR MUX which selects one of the 8 available taps of the prescaler outputs under the control of PSC0,1,2 in the AR Mode Control Register (address D5h). So the division factor of PSC prescaler can be set to 2^n (where n = 0, 1...7).

The clock input to the TC counter is enabled by bit TEN (Timer Enable) in the Status Control Register 1. When TEN is cleared to "0" the TC counter is stopped and the prescaler and counter contents are frozen. When the TEN bit is set to "1" the TC counter runs at the rate of the selected clock source. TC is cleared after system reset.

The ARTC counter can also be initialized by writing into the load register ARLR, which causes also the immediate copy of the value into the ARTC counter regardless of whether ARTC is running or not. Initialization of ARTC, in both ways, will also clear the ARPSC in order to start counting from a known state.

Each interrupt generated by the AR Timer operating modes is associated to interrupt vector #3.

Timer Operating Modes

Four different operating modes are available for the AR Timer:

Auto-reload Mode with PWM Generation. This mode allows a Pulse Width Modulated signal to be generated on the ARTIMout output pin with minimum Core processing time used.

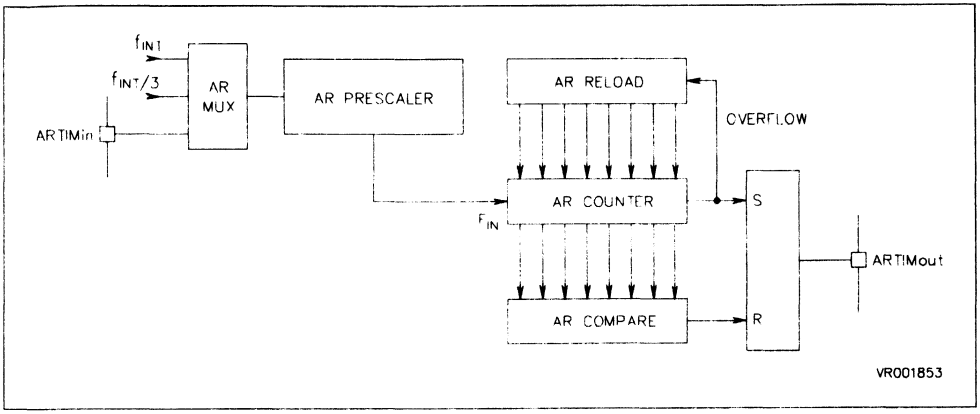
ARTC is a free running 8-bit counter fed by the ARPSC prescaler output and is incremented on every rising edge of the clock signal.
When a counter overflow occurs the ARTC counter is automatically reloaded with the contents of the Reload Register (ARRC, address D9h) while ARTIMout is set. When the counter reaches the value contained in the compare register ARCP, ARTIMout is reset.

At overflow, an overflow interrupt request is generated if the overflow interrupt enable bit, OVIE in the mode control register (ARMC, address D5h), is set to "1".
When the counter reaches the compare value a compare interrupt request is generated if the Compare Interrupt enable bit, CPIE, in the Mode Control Register (ARMC, address D5h), is set to one. The interrupt service routine may then adjust the PWM period by loading a new value into ARCP.

The PWM signal is generated at ARTIMout (refer to block diagram) connected to the ARTIMout output pin. The frequency of this signal is controlled by the prescaler and by the auto-reload value present in the Reload/Capture register ARRC (address D9h). The duty cycle of the PWM signal is controlled by the Compare Register (ARCP, address DAh).

TIMERS (Continued)

Figure 33. Auto-reload Timer Block Diagram



Note that the reload values will also affect the value and the resolution of the duty cycle of PWM output signal. To achieve a ARTIMout signal the contents of the ARCP register must be greater than the contents of the ARRC register.

The maximum available resolution for the ARTIMout duty cycle is:

Resolution = 1/[255-(ARRC)]

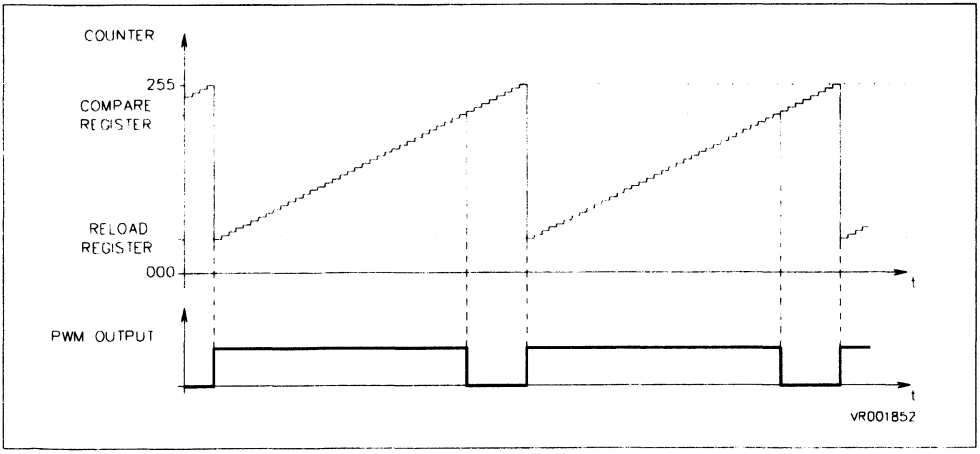
Where ARRC is the content of Reload/Capture register and the compare value loaded in the Compare Register, ARCP, must be in the range from (ARRC) to 255.

The initialization of the ARTC counter is made by writing into the ARRC register, then by setting the TCLD (Timer Load) and the TEN (Timer Clock Enable) bits in the Mode Control register ARMC.

The enable and the selection of clock sources are controlled by CC0, CC1, SL0 and SL1 bits in the Status Control Register ARSC1. The prescaler division ratio is selected by PS0, PS1 and PS2 bits in the ARSC1 Register.

In Auto-reload Mode any clock source can be selected: Internal Clock, Internal Clock divided by 3 or the signal at the ARTIMin input pin.

Figure 34. Auto-reload Timer PWM Function



TIMERS (Continued)

Capture Mode with PWM Generation. In this case, ARTC is a free running 8-bit counter fed by the PSC prescaler output. ARTC is incremented on every clock rising edge.

An 8-bit capture operation from ARTC counter to ARRC register is performed on every active edge at ARTIMin/PC Input pin when enabled by Edge Control bits SL0, SL1 in the ARSC1 register. At the same time the External Flag EF, in the SC0 register, is set and an external interrupt request is generated if the External Interrupt Enable bit EIE, in the ARMC register, is set to one.

Each ARTC overflow sets ARTIMout, while a match between ARTC and ARCP (Compare Register) contents resets ARTIMout and sets the compare flag ARCPF and the compare interrupt request is generated if the related compare interrupt enable bit CPIE is set. A PWM signal is generated at ARTIMout.

The frequency of this signal is controlled by the prescaler. The duty cycle is controlled by register ARCP from 0-255/256.

Initialization and reading of ARTC counter are made in the same way as in the auto-reload mode (see previous paragraph).

The enable and selection of clock sources is controlled by CC0, CC1 bits in the AR Status Control Register ARSC1.

The prescaler division ratio is selected by PS0, PS1 and PS2 bits in the ARSC1 Register.

In Capture mode the possible clock sources are the internal clock and the internal clock divided by 3; the external ARTIMin input pin should not be used.

Capture Mode with Reset of ARTC, ARPSC and PWM Generation. This mode is identical to the previous one, with the difference that a capture condition also resets the ARTC counter and ARPSC prescaler allowing easy measurement of the time between two captures (for input period measurement on ARTIMin pin).

Load on External Input. ARTC is a free running 8-bit counter fed by the ARPSC prescaler. TC is incremented on every clock rising edge.

Each ARTC overflow sets the ARTIMout. A match between ARTC and ARCP (Compare Register) contents resets the ARTIMout and sets the compare flag CPF and the compare interrupt request is generated if the related compare interrupt enable bit CPIE is set. A PWM signal is generated at ARTIMout.

The initialization of ARTC can be done in the same way as described in the previous paragraph. In addition if the external ARTIMin input is enabled, an active edge on the input pin will copy the contents of the ARRC register into the ARTC counter, whether ARTC is running or not.

General Notes:

a - The allowed AR Timer clock sources are the following:

AR Timer mode	Clock Sources
Auto-reload mode	f_{INT}, $f_{INT}/3$, ARTIMin
Capture mode	f_{INT}, $f_{INT/3}$
Capture/Reset mode	f_{INT}, $f_{INT/3}$
External Load mode	f_{INT}, $f_{INT/3}$

b - The timer clock frequency should not be modified while ARTC is counting as the ARTC counter may take an unpredictable value. For example the multiplexer setting should not be modified while ARTC is counting.

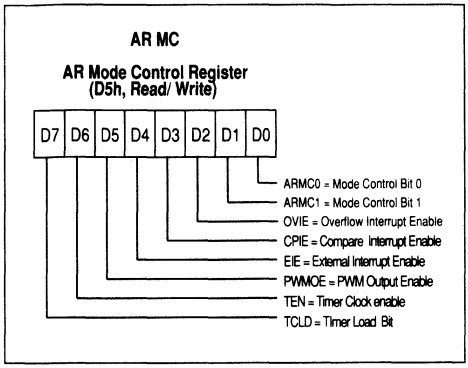
c - Any loading of ARTC (by auto-reload, through ARLR, ARRC or by the Core) resets ARPSC at the same time.

TIMERS (Continued)

AR Timer Registers

Mode Control Register ARMC. The AR Mode Control Register ARMC is used to program the different operation modes of AR Timer, to enable the clock of the Timer/Counter and to initialize it. It can be read and written by the Core and it is cleared to zero on system reset (AR Timer is disabled).

Figure 35. AR Mode Control Register



TCLD. This bit, when set to one, will cause the contents of ARRC register to be loaded into the ARTC counter and the contents of ARPSC register are cleared in order to initialize the timer before starting to count. This bit is write only and any attempt to read it will show a logical zero.

TEN. This bit, when set to one, will allow the timer to count. When cleared to zero it will stop the timer and freeze the ARPSC and ARTSC values.

PWMOE. This bit, when set, enables the PWM output to be carried on ARTIMout output pin. When cleared to zero the PWM output is disabled.

EIE. This bit, when set, enables the external interrupt request. If EIE = "0" the external interrupt request is masked. If EIE = "1" and the related flag EF in the ARSC0 register is also set an interrupt request is generated.

CPIE. This bit, when set, enables the compare interrupt request. If CPIE = "0" the compare interrupt request is masked. If CPIE = "1" and the related flag CPF into the ARSC0 register is also set an interrupt request is generated.

OVIE. This bit, when set, enables the overflow interrupt request. If OVIE = "0" the compare interrupt request is masked. If OVIE = "1" and the related flag OVF into the ARSC0 register is also set, an interrupt request is generated.

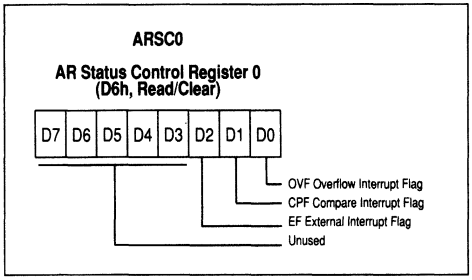
ARMC1, ARMC0. These are the operation mode control bits. The following bit combination will select the different operating modes:

ARMC1	ARMC0	Operating Mode
0	0	Auto-reload Mode
0	1	Capture Mode
1	0	Capture Mode with Reset of ARTC and ARPSC
1	1	Load on External Edge Mode

AR Timer Status/Control Registers ARSC0 & ARSC1. These registers provide the AR Timer status information bits and also allows the programming of clock sources, active edge and prescaler multiplexer programming.

ARSC0 register bits 0,1 and 2 contains the interrupt flags of the AR Timer. These bits can read and cleared by the Core. A normal write operation is not possible, it is only possible to reset the bits by writing a zero on the selected position. Writing a one will not affect the bit flag bits.

Figure 36. AR Status Control Register 0



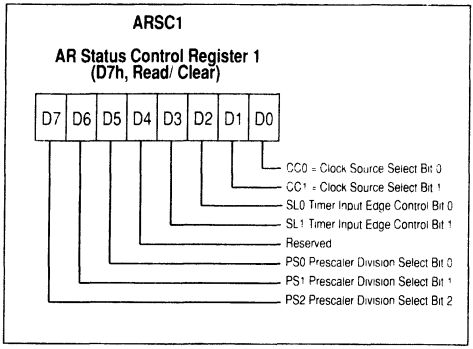
EF. This bit is set to one by any active edge at the external ARTIMin input pin. The flag is cleared by writing a zero in the EF bit.

CPF. This bit is set to one if the contents of ARTC counter and ARCP register are equal. The flag is cleared by writing a zero into ARCPF bit.

OVF. This bit is set to one by a transition of TC counter from FFh to 00h. The flag is cleared by writing a zero into OVF bit.

TIMERS (Continued)

Figure 37. AR Status Control Register 1



PS2-PS0. These bits control the AR Prescaler division ratio. The prescaler itself is not affected by these bits. The AR PSC division is listed in the following Table 10:

Table 10. Prescaler Division Ratio Selection

PS2	PS1	PS0	ARPSC Division Ratio
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

D4. Reserved. Must be kept to 0.

SL1-SL0. These bits control the edge function on AR Timer input pin for external synchronization. If bit SL0 is cleared to zero the edge detection is disabled, if set to one the edge detection is enabled. If bit SL1 is cleared to zero the AR Timer input pin is rising edge sensitive, if set to one it is falling edge sensitive.

SL1	SL0	Edge Detection
X	0	Disabled
0	1	Rising Edge
1	1	Falling Edge

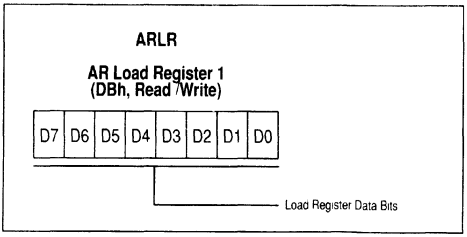
CC1-CC0. These bits select the clock source for the AR Timer through the AR Multiplexer. The programming of the clock sources is explained in the following Table 11:

Table 11. Clock Source Selection

CC1	CC0	Clock Source
0	0	Core Clock
0	1	Core Clock Divided by 3
1	0	ARTIMin Input Clock
1	1	Reserved

AR Load Register ARLR. The ARLR load register is used to read or write "on the fly" the ARTC counter register, while it is counting. ARLR register is not affected by system reset.

Figure 38. AR Load Register

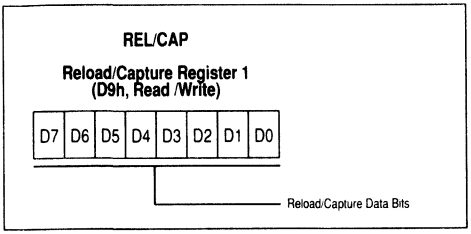


D7-D0. These are the load register data bits.

TIMERS (Continued)

AR Reload/Capture Register. The ARRC reload/capture register is used to hold the auto-reload value that is automatically loaded into ARTC counter from ARRC when overflow occurs.

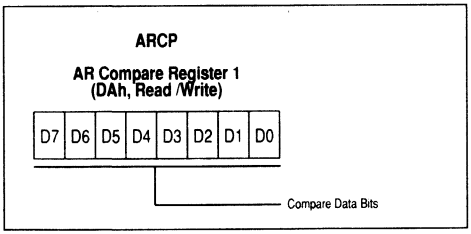
Figure 39. AR Reload/Capture



D7-D0. These are the Reload/Capture register data bits.

AR Compare Register. The CP compare register is used to hold the compare value to perform the compare function with TC counter.

Figure 40. AR Compare Register



D7-D0. These are the Compare register data bits.

Synchronization

The clock of the counter, the capture and reload operations and the reading of the reload/capture register are triggered by independent asynchronous sources. To prevent capture of a transient counter content or a reading of transient capture value the different sources are synchronized internally by the AR Timer synchronization logic. The Clock and Trigger sources, AR Timer Input and internal clock are synchronized with the processor read/write strobes. To avoid any loss of clock or trigger pulses the frequency of the external signal should be equal to or lower than 1/4 of the internal clock.

DIGITAL WATCHDOG

The digital Watchdog of the ST6260/65 device consists of a down counter that can be used to provide a controlled recovery from a software upset.

The Watchdog generates a system reset when the counter passes 00h. User software can prevent the reset by reloading the counter. User software should therefore be written in such a way that the counter is regularly reloaded as long as the software runs correctly. In the case of software upset (e.g. infinite loop or power supply fail), user software should not reload the counter so it will pass 00h and reset the MCU.

The Watchdog activation (hardware or software) is user selectable by mask option. If the hardware option is selected the Watchdog is automatically initialized after reset so that this function does not need to be activated by the user program. STOP mode is not available when hardware activation is selected. In case of software option the Watchdog activation is controlled by the user software. If the watchdog is not activated, the STOP mode is available and the watchdog counter can be used as a timer.

The Watchdog uses one data space register (DWDR location D8h). The Watchdog register is set to FEh on reset and immediately starts to count down, requiring no software start if the hardware option has been selected. The Watchdog time canbe adjusted through the value reloaded into the DWDR register. Only the 6 MSbits are significant.

This gives the possibility to generate a reset in a time between 3072 to 196608 clock cycles in 64 possible steps: (With a clock frequency of 8MHz this means from 384µs to 24.576ms). The reset is prevented if the register is reloaded before bits 2-7 decrement from all zeros to all ones. If the software option is selected and the watchdog not activated, the 7 MSbits of the counter can be used to perform timer functions.

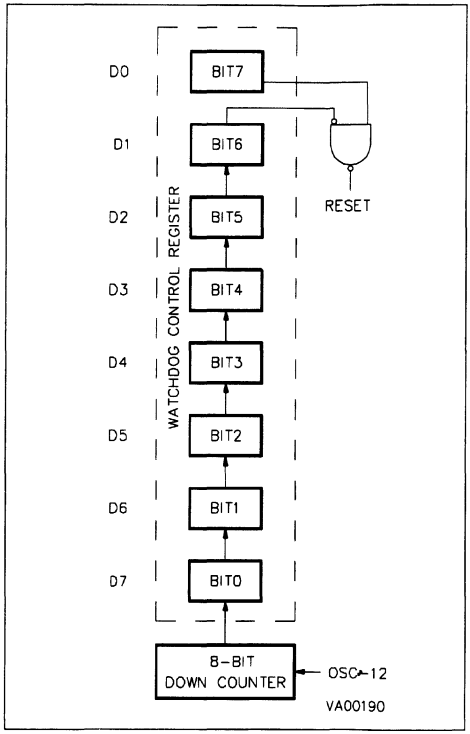
Note:

Care must be taken when using the software Watchdog as a timer as the Watchdog bits are in reverse order.

If the Watchdog is active (independent of the watchdog option) the STOP instruction is deactivated and a WAIT instruction is automatically executed instead of a STOP. Bit 1 of the Watchdog register (set to one at reset) can be used to generate a software reset if cleared to zero.

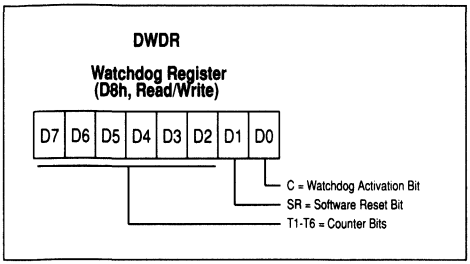
If the software option is selected, after a reset, the Watchdog is in the off-state. The Watchdog can be activated by setting bit 0 of the DWDR register after bit SR has been set to one. Once bit 0 is set, it cannot be cleared by software. It is cleared by a reset.

Figure 41. Watchdog Working Principle



DIGITAL WATCHDOG (Continued)

Figure 41. Digital Watchdog Register



C. This is the Watchdog activation bit. If hardware option is selected, it is forced high and the user cannot change it (the Watchdog is always active). When the software option is selected, the Watchdog function is activated by setting C to 1. It can then be cleared only by a system reset. When C is kept low the counter can be used as a 7-bit timer.

When cleared to zero it allows the use of the counter as a 7-bit timer. This bit is cleared on reset.

SR. This bit is set to one during the reset and will generate a software reset if cleared to zero. When C = "0" (watchdog disabled) it is the MSB of the 7-bit timer.

T1-T6. These are the watchdog counter bits. It must be noted that D7 (T1) is the LSB of the counter and D2 (T6) is the MSB of the counter.

Application note:

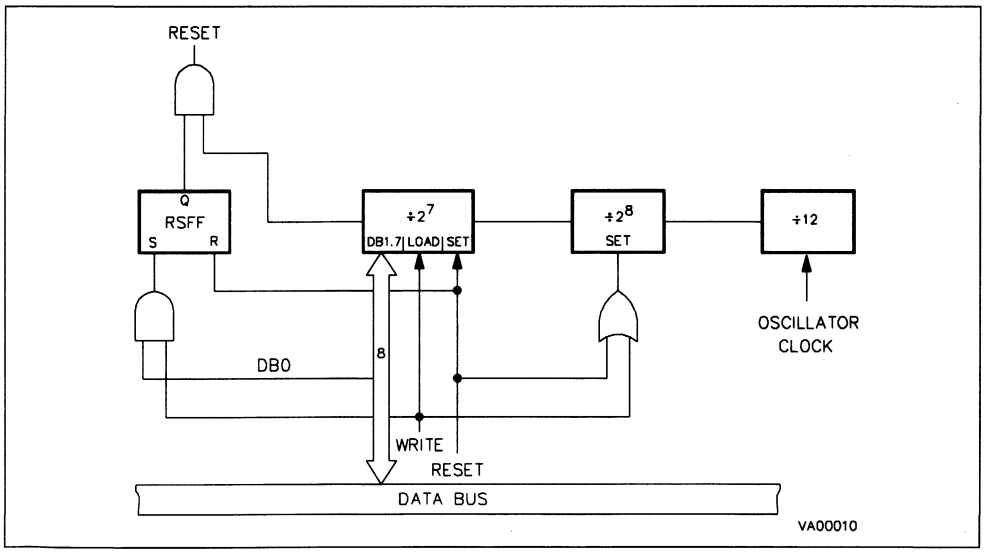
The watchdog has an inportant role in the high noise immunity of the ST62 devices. It should therefore be used unless the STOP mode is required. When the watchdog is used, the hardware activation should be prefered as it provides maximum security, especially during power on. With all modes, a minimum of 28 instructions are executed after activation before the watchdog can generate a reset. Consequently, user software must reload the watchdog counter within the first 27 instructions following watchdog activation (software mode) or the first 27 instructions executed after a reset (hardware activation).

Software activation should be used only when the STOP mode is required or the watchdog counter must be used as timer. To ensure the watchdog has not been unexpectantly turned on, the following instructions should be executed within the first 27 instructions.

```
jrr 0, WD, #+3
ldi WD, 0FDH
```

These instructions test the C bit and reset it (i.e. deactivate the watchdog) if relevant (i.e. if the watchdog is active) by performing a software reset.

Figure 42. Digital Watchdog Block Diagram



8-BIT A/D CONVERTER

The A/D converter of ST6260/65 device is an 8-bit analog to digital converter with up to 7 (ST6260) and up to 13 (ST6265) analog inputs (as alternate functions of I/O lines PA0-PA7, PC0-PC3) offering 8-bit resolution with total accuracy ±2 LSB and a typical conversion time of 70µs (clock frequency of 8MHz).

The A/D peripheral converts the input voltage by a process of successive approximations using a clock frequency derived from the oscillator with a division factor of twelve. With an oscillator clock frequency less than 1.2MHz, the A/D converter accuracy is decreased.

The selection of the pin signal that has to be converted is done by configuring the related I/O line as analog input through the I/O ports option and data registers (refer to I/O ports description for additional information). Only one I/O line must be configured as analog input at a time. The user must avoid the situation in which more than one I/O pin is selected to be analog input to avoid malfunction of the ST62xx.

The ADC uses two registers in the data space: the ADC data conversion register which stores the conversion result and the ADC control register used to program the ADC functions.

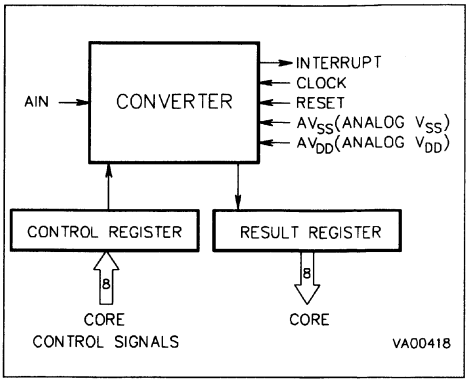
A conversion is started by writing a "1" to the Start bit (STA) in the ADC control register. This automatically clears (resets to "0") the End Of Conversion Bit (EOC). When a conversion has been finished this EOC bit is automatically set to "1" in order to flag that conversion is complete and that the data in the ADC data conversion register is valid. Each conversion has to be separately initiated by writing to the STA bit.

The STA bit is continually being scanned so that if the user sets it to "1" while a previous conversion is in progress then a new conversion is started before the previous one has been completed.The start bit (STA) is a write only bit, any attempt to read it will show a logical "0".

The A/D converter has a maskable interrupt associated to the end of conversion. This interrupt is associated to the interrupt vector #4 and occurs when the EOC bit is set, i.e. when a conversion is completed. The interrupt is masked using the EAI (interrupt mask) bit in the control register.

The power consumption of the device can be reduced by turning off the ADC peripheral. That is achieved when the PDS bit in the ADC control register is cleared to "0". If PDS="1", the A/D is supplied and enabled for conversion. This bit must be set at least one instruction before the beginning of the conversion to allow the stabilization of the

Figure 43. A/D Converter Block Diagram



A/D converter. *This action is needed also before entering the STOP instruction as the A/D comparator is not automatically disabled by the STOP mode*

During reset any conversion in progress is stopped, the control register is reset to all zeros and the A/D interrupt is masked (EAI=0).

Notes:

The ST62xx A/D converter does not feature a sample and hold. The analog voltage to be measured should therefore be stable during the conversion time. Variation should not exceed ±1/2 LSB for the best accuracy in measurement.

Since the ADC is on the same chip as the microprocessor the user should not switch heavily loaded output signals during conversion if high precision is needed. This is because such switching will affect the supply voltages which are used for comparisons.

A low pass filter can be used at the analog input pins to reduce input voltage variation during the conversion. For true 8 bit conversions the impedance of the analog voltage sources should be less than 30kΩ while the impedance of the reference voltage should not exceed 2kΩ.

The accuracy of the conversion depends on the quality of the power supply voltages (V_{DD} and V_{SS}). The user must specially take care of applying regulated reference voltage on the V_{DD} and V_{SS} pins (the variation of the power supply voltage must be inferior to 5V/ms).

The converter can resolve the input voltage with a resolution of:

$$\frac{V_{DD} - V_{SS}}{256}$$

8-BIT A/D CONVERTER (Continued)

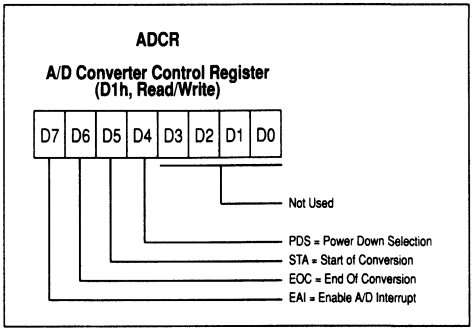
The Input voltage (Ain) which has to be converted must be constant for 1µs before conversion and remain constant during the conversion.

The resolution of the conversion can be improved if the power supply voltage (V_{DD}) of the microcontroller becomes lower.

In order to optimize the resolution of the conversion, the user can configure the microcontroller in the WAIT mode because this mode allows the minimization of the noise disturbances and the variations of the power supply voltages due to the switching of the outputs. Nevertheless, it must be take care of executing the WAIT instruction as soon as possible after the beginning of the conversion because the execution of the WAIT instruction may provide a small variation of the V_{DD} voltage (the negative effect of this variation is minimized at the beginning of the conversion because the latter is less sensitive than the end of the conversion when the less significant bits are determined).

The best configuration from a accuracy point of view is the WAIT mode with the Timer and LCD driver stopped. Indeed, only the ADC peripheral and the oscillator are still working. The MCU has to be wake-up from the WAIT mode by the interrupt of the ADC peripheral at the end of the conversion. It must be noticed that the wake-up of the microcontroller could be done also with the interrupt of the TIMER, but in this case, the Timer is working and some noise could disturb the converter in terms of accuracy.

Figure 44. A/D Converter Control Register



EAI. If this bit is set to one the A/D interrupt (vector #4) is enabled, when EAI=0 the interrupt is disabled.

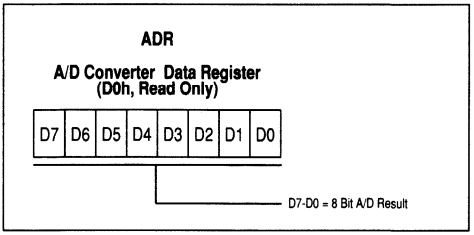
EOC. *Read Only*;This read only bit indicates when a conversion has been completed. This bit is automatically reset to zero when the STA bit is written. If the user is using the interrupt option then this bit can be used as an interrupt pending bit. Data in the data conversion register are valid only when this bit is set to one.

STA. *Write Only*; Writing a "1" in this bit will start a conversion on the selected channel and automatically reset to zero the EOC bit. If the bit is set again when a conversion is in progress, the present conversion is stopped and a new one will take place. This bit is write only, any attempt to read it will show a logical zero.

PDS. This bit activates the A/D converter if set to "1". Writing a zero into this bit will put the ADC in power down mode (idle mode).

D3-D0. Not used

Figure 45. A/D Converter Data Register



SERIAL PERIPHERAL INTERFACE SPI

The ST6260/65 SPI is an optimized synchronous serial interface with programmable transmission modes and master/slave capabilities supporting a wide range of industry standard SPI specifications. The ST6260/65 SPI is controlled by simple user software to perform serial data exchange with low-cost external memory or serially controlled peripherals for display or driving motors or relays. The peripheral is composed of an 8-bit data/shift register DSR (address E0h), by a Divide register DIV (address E1h) and by a mode control register MOD (address E2h).

The SPI may be used as either a Master or a Slave Unit. The Master is defined by the synchronous serial clock line SCK being supplied by the MCU, while the Slave mode accepts external data with the SCK clock externally supplied. For the Master mode of the SPI, SCK is internally generated with a frequency derived from a programmable division ratio of the Oscillator Clock divided by 13. Input may also be disabled in Master mode for data security.

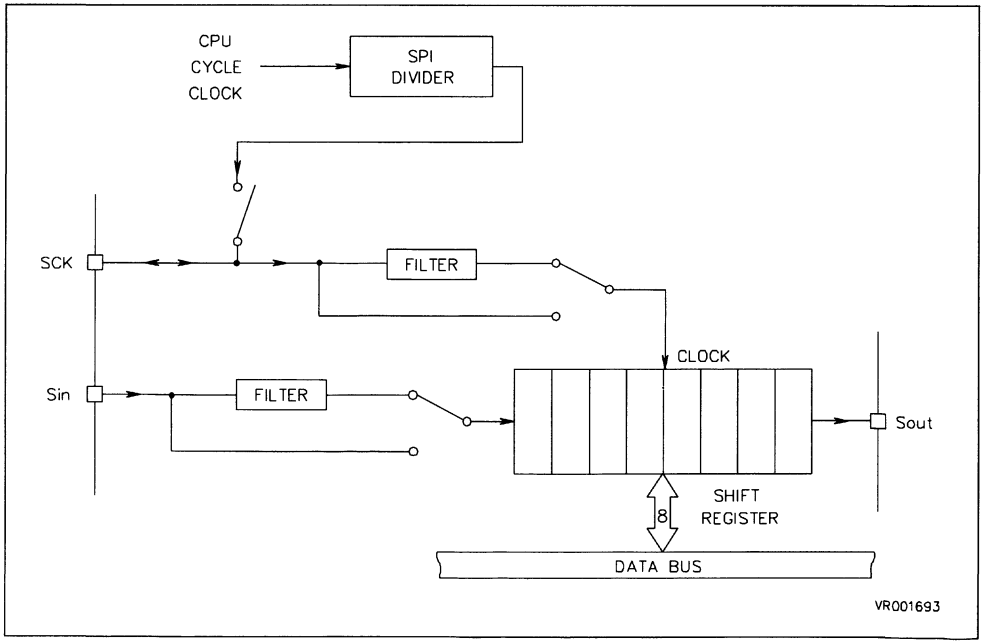
For maximum versatility the SPI be programmed to sample the synchronous data for transmit and receive on the rising or falling edge of SCK, and with or without a phase shift.

The Sin, Sout and SCK (SPI Data in, Data out and Clock signals respectively) signals are connected, as alternate functions, to I/O pins PC2-PC4. PC2 is connected with the SPI Serial Data Input Sin, PC3 is connected with the SPI Serial Data Output Sout and PC4 is connected with the SPI Clock Input/Output SCK.

For serial input operation PC2/Sin must be programmed as input. For serial output operation, PC3/Sout alternate function is selected by programming Bit 0 of Miscellaneous Register (address DDh); writing a zero will set the pin as PC3 I/O line while writing a one will select the SPI Sout functionality. The serial clock Input mode is selected if the PC4 port pin is programmed in input mode and bit SPCLK is cleared. The output mode is selected if PC4 is programmed in output mode and SPCLK is set to 1.

An interrupt request can be associated to the end of transmission. This request is associated to interrupt vector #4 and can be masked by programming bit SPIE of the SPI MOD register. As the SPI interrupt is "ORed" with Port C interrupt source, an interrupt flag bit is available in the DIV register allowing the discrimination of the interrupt request.

Figure 46. SPI Block Diagram



SERIAL PERIPHERAL INTERFACE SPI (Continued)

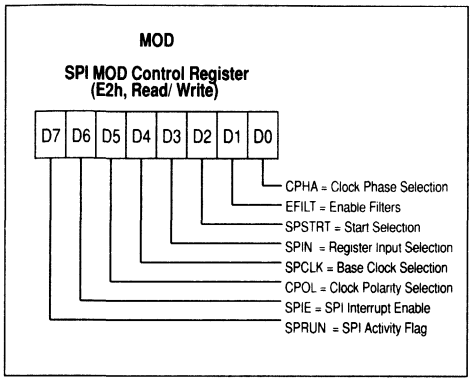
SPI Registers

SPI MODE (SPIMOD) Control Register

The MOD control register defines and controls the transmission modes and characteristics.

This register is read/write and all bits are cleared at reset. The configuration of SPSTRT = 1 and SPIN = 1 is not allowed and must be avoided.

Figure 47. SPI MOD Control Register



SPRUN. This bit is the SPI activity flag. This can be used in either read or write modes; it is automatically cleared by the SPI at the end of a transmission and generates an interrupt request (providing that the SPIE Interrupt Enable bit is set). The Core can stop the running transmission at any time by resetting the SPRUN bit; this will also generate an interrupt request (providing that the SPIE Interrupt enable bit is set). The SPRUN bit can be used as the start bit, in conjunction with the SPSTRT bit, when an external signal is present on the Sin pin.

SPIE. This bit is the SPI Interrupt Enable bit. If this bit is set to one the SPI interrupt (vector #4) is enabled, when SPIE = "0" the interrupt is disabled.

CPHA. This bit selects the clock phase of the clock signal. If this bit is cleared to zero the normal state is selected; in this case Bit 7 of the data frame is present on Sout pin as soon as the SPI Shift Register is loaded. If this bit is set to one the shifted state' is selected; in this case Bit 7 of data frame is present on Sout pin on the first falling edge of Shift Register clock. The polarity relation and the division ratio between Shift Register and SPI base clock are also programmable; refer to DIV register and Timing Diagrams for more information.

SPCLK. This bit selects the SPI base clock source. It is either the core cycle clock ($f_{INT}/13$) (Master mode) or the signal provided at SCK pin by an external device (slave mode). If SPCLK is low and the SCK pin is configured as input, the slave mode is selected. If SPCLK is high and the SCK pin is configured as output, the master mode is selected. In this case, the phase and polarity of the clock are controlled by CPOL and CPHA.

SPIN. This bit enables the transfer of the data input to the Shift Register in received mode. If this bit is cleared to zero the Shift Register input is 0. If this bit is set to one the Shift Register input corresponds to the input signal present on the Sin pin.

SPSTRT. This bit selects the transmission start mode. If this bit is cleared to zero the internal start condition occurs as soon as the SPRUN bit is enabled (set to one). If this bit is set to one, the internal start signal is the logic "AND" between the SPRUN bit and the external signal present on the Sin pin; in this case transmission will start after the latest of both signals providing that the first signal is still present. After the transmission has been started, it will continue even if the Sin signal is reset.

EFILT. This bit enables/disables the input noise filters on the Sin and SCK inputs. If it is cleared to zero the filters are disabled, if set to one the filters are enabled. These noise filters will eliminate any pulse on Sin and SCK with a pulse width smaller than one to two Core clock periods (depending on the occurrence of the signal edge with respect to the Core clock edge). For example, if the ST6260/65 runs with an 8MHz crystal, Sin and SCK will be delayed by 125 to 250ns.

CPOL. This bit controls the relationship between the data on the Sin and Sout pins and SCK. The CPOL bit selects the clock edge which captures data and allows it to change state. It has the greatest impact on the first bit transmitted (the MSB) as it does (or does not) allow a clock transition before the first data capture edge.

Refer to the timing diagrams at the end of this section for additional details. These show the relationship between CPOL, CPHA and SCK, and indicate the active clock edges and strobe times.

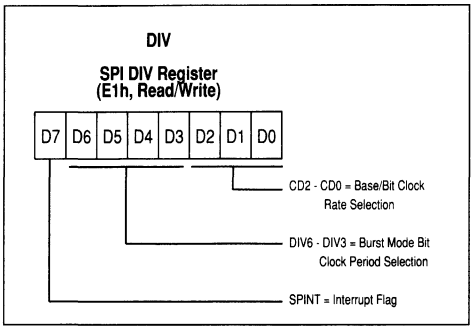
SERIAL PERIPHERAL INTERFACE SPI (Continued)

SPI Divide (SPIDIV) Register

The SPIDIV register defines the SPI transmission rate and frame format. It also contains the interrupt flag bit.

Bits CD0-CD2, DIV3-DIV6 are read/write while SPINT can be read and cleared only. Write access is not allowed if the SPRUN bit of Mode Control register is set to one. All bits are cleared at reset.

Figure 48. SPI DIV Register



SPINT/DIV7. This is the SPI interrupt flag bit. It is automatically set to one by the SPI at the end of a transmission and an interrupt request can be generated in accordance with the state of the interrupt mask bit into the MOD control register. This bit is read only and has to be cleared by the user software at the end of the interrupt service routine.

DIV6-DIV3. These bits define the number of shift register bits that are transmitted in a transmission frame. The available selections are listed in Table 13. The normal setting for is for 8 bits.

CD2-CD0. These bits define the division ratio between the core clock (f_{INT}divided by 13) and clock supplied to the Shift Register in Master mode.

Table 12. Base/Bit Clock Ratio Selection

CD2-CD0	Divide Ratio (decimal)
0 0 0	Divide by 1
0 0 1	Divide by 2
0 1 0	Divide by 4
0 1 1	Divide by 8
1 0 0	Divide by 16
1 0 1	Divide by 32
1 1 0	Divide by 64
1 1 1	Divide by 256

Table 13. Burst Mode Bit Clock Periods

DIV6-DIV3	Divide Ratio (decimal)
0 0 0 0	Reserved (not to be used)
0 0 0 1	Divide by 1
0 0 1 0	Divide by 2
0 0 1 1	Divide by 3
0 1 0 0	Divide by 4
0 1 0 1	Divide by 5
0 1 1 0	Divide by 6
0 1 1 1	Divide by 7
1 0 0 0	Divide by 8
1 0 0 1	Divide by 9
1 0 1 0	Divide by 10
1 0 1 1	Divide by 11
1 1 0 0	Divide by 12
1 1 0 1	Divide by 13
1 1 1 0	Divide by 14
1 1 1 1	Divide by 15

SPI Data Shift (DSR) Register

SPIDSR is the SPI data shift register.

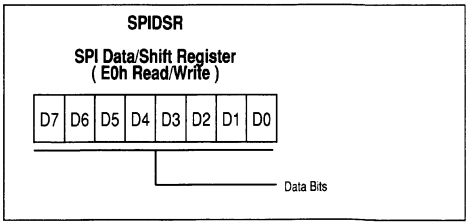
The Shift Register transmits and receives the Most Significant bit as the first bit.

SPIDSR is read/write, however write access is not allowed if the SPRUN bit of Mode Control register is set to one.

DSR7-DSR0. These are the SPI shift register data bits.

Data is sampled into DSR on the SCK edge determined by the CPOL and CPHA bits. The affect of these setting is shown in the following diagrams.

Figure 49. SPI Data/Shift Register



SERIAL PERIPHERAL INTERFACE SPI (Continued)

SPI Timing Diagrams

Figure 50. CPOL = 1 Clock Polarity Inverted, CPHA = 0 Phase Selection Normal

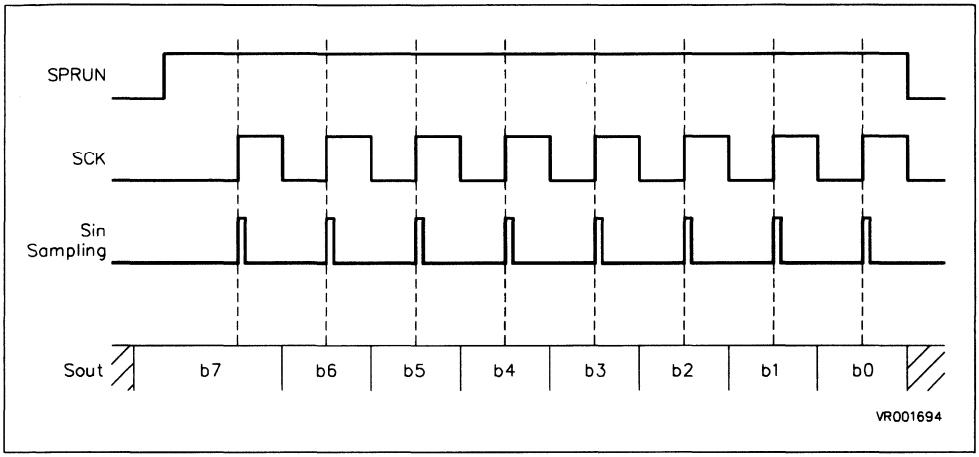
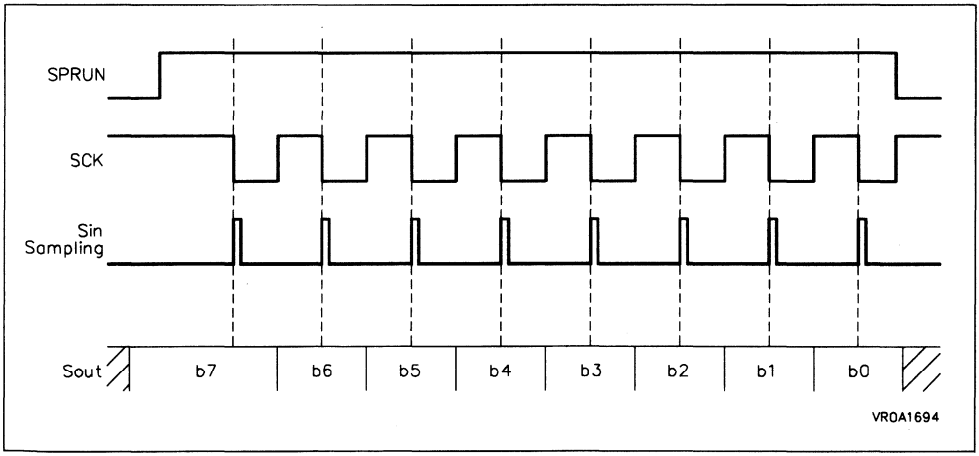


Figure 51. CPOL = 0 Clock Polarity Normal, CPHA = 0 Phase Selection Normal



SERIAL PERIPHERAL INTERFACE (Continued)

Figure 52. CPOL = 0 Clock Polarity Normal, CPHA = 1 Phase Selection Shifted

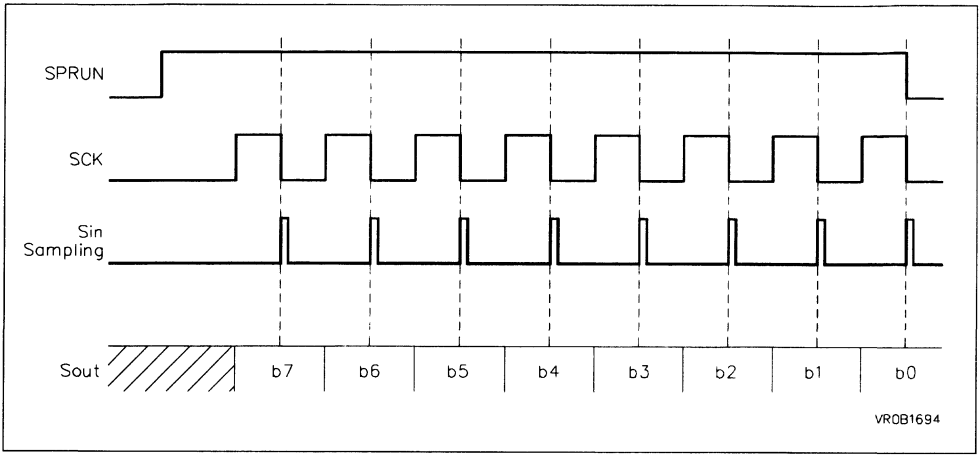
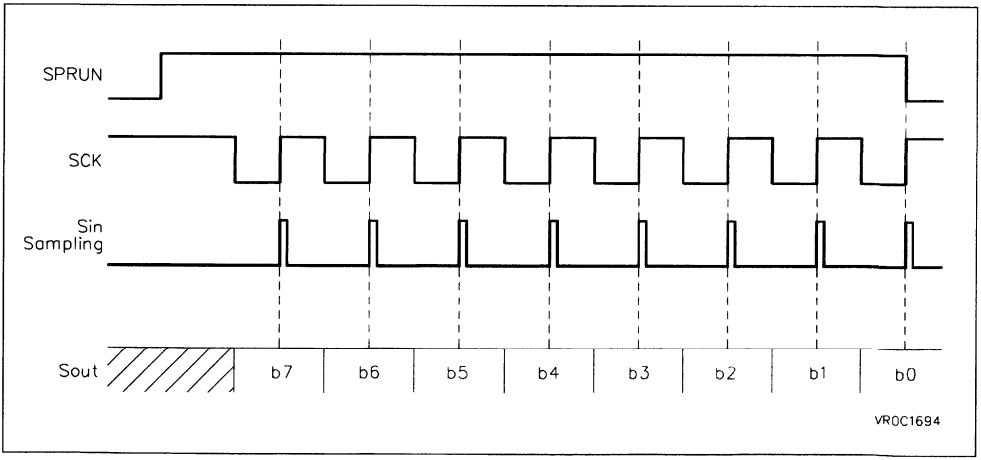


Figure 53. CPOL =1 Clock Polarity Inverted CPHA = 1 Phase Selection Shifted



SOFTWARE DESCRIPTION

The ST62xx software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short to provide byte efficient programming capability. The ST62xx core has the ability to set or clear any register or RAM location bit of the Data space with a single instruction. Furthermore, the program may branch to a selected address depending on the status of any bit of the Data space. The carry bit is stored with the value of the bit when the SET or RES instruction is processed.

Addressing Modes

The ST62xx core has nine addressing modes which are described in the following paragraphs. The ST62xx core uses three different address spaces : Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, plus the data for immediate mode instructions. Data space contains the Accumulator, the X,Y,V and W registers, peripheral and Input/Output registers, the RAM locations and Data ROM locations (for storage of tables and constants). Stack space contains six 12-bit RAM cells used to stack the return addresses for subroutines and interrupts.

Immediate. In the immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In the direct addressing mode, the address of the byte that is processed by the instruction is stored in the location that follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data Space memory with a single two-byte instruction.

Short Direct. The core can address the four RAM registers X,Y,V,W (locations 80h, 81h, 82h, 83h) in the short-direct addressing mode . In this case, the instruction is only one byte and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of the direct addressing mode. (Note that 80h and 81h are also indirect registers).

Extended. In the extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four less significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) that use the extended addressing mode are able to branch to any address of the 4K bytes Program space.

An extended addressing mode instruction is two-byte long.

Program Counter Relative. The relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to +16 locations around the address of the relative instruction. If the condition is not true, the instruction that follows the relative instruction is executed. The relative addressing mode instruction is one-byte long. The opcode is obtained in adding the three most significant bits that characterize the kind of the test, one bit that determines whether the branch is a forward (when it is 0) or backward (when it is 1) branch and the four less significant bits that give the span of the branch (0h to Fh) that must be added or subtracted to the address of the relative instruction to obtain the address of the branch.

Bit Direct. In the bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 locations of Data space memory can be set or cleared.

Bit Test & Branch. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit test and branch instruction is three-byte long. The bit identification and the tested condition are included in the opcode byte. The address of the byte to be tested follows immediately the opcode in the Program space. The third byte is the jump displacement, which is in the range of -126 to +129. This displacement can be determined using a label, which is converted by the assembler.

Indirect. In the indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed by the content of one of the indirect registers, X or Y (80h,81h). The indirect register is selected by the bit 4 of the opcode. A register indirect instruction is one byte long.

Inherent. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

SOFTWARE DESCRIPTION (Continued)

Instruction Set

The ST62xx core has a set of 40 basic instructions. When these instructions are combined with nine addressing modes, 244 usable opcodes can be obtained. They can be divided into six different types:load/store, arithmetic/logic, conditional branch, control instructions, jump/call, bit manipulation. The following paragraphs describe the different types.

All the instructions within a given type are presented in individual tables.

Load & Store. These instructions use one,two or three bytes in relation with the addressing mode. One operand is the Accumulator for LOAD and the other operand is obtained from data memory using one of the addressing modes.

For Load Immediate one operand can be any of the 256 data space bytes while the other is always immediate data.

Table 14. Load & Store Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
LD A, X	Short Direct	1	4	Δ	*
LD A, Y	Short Direct	1	4	Δ	*
LD A, V	Short Direct	1	4	Δ	*
LD A, W	Short Direct	1	4	Δ	*
LD X, A	Short Direct	1	4	Δ	*
LD Y, A	Short Direct	1	4	Δ	*
LD V, A	Short Direct	1	4	Δ	*
LD W, A	Short Direct	1	4	Δ	*
LD A, rr	Direct	2	4	Δ	*
LD rr, A	Direct	2	4	Δ	*
LD A, (X)	Indirect	1	4	Δ	*
LD A, (Y)	Indirect	1	4	Δ	*
LD (X), A	Indirect	1	4	Δ	*
LD (Y), A	Indirect	1	4	Δ	*
LDI A, #N	Immediate	2	4	Δ	*
LDI rr, #N	Immediate	3	4	*	*

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr. Data space register
Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Arithmetic and Logic. These instructions are used to perform the arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while the other can be either a data space memory content or an immediate value in relation with the addressing mode. In CLR, DEC, INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator.

Table 15. Arithmetic & Logic Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	*
AND A, (Y)	Indirect	1	4	Δ	*
AND A, rr	Direct	2	4	Δ	*
ANDI A, #N	Immediate	2	4	Δ	*
CLR A	Short Direct	2	4	Δ	Δ
CLR r	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
. Immediate data (stored in ROM memory)
rr. Data space register
Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Conditional Branch. The branch instructions achieve a branch in the program when the selected condition is met.

Bit Manipulation Instructions. These instructions can handle any bit in data space memory. One group either sets or clears. The other group (see Conditional Branch) performs the bit test branch operations.

Control Instructions. The control instructions control the MCU operations during program execution.

Jump and Call. These two instructions are used to perform long (12-bit) jumps or subroutines call inside the whole program space.

Table 16. Conditional Branch Instructions

Instruction	Branch If	Bytes	Cycles	Flags	
				Z	C
JRC e	C = 1	1	2	*	*
JRNC e	C = 0	1	2	*	*
JRZ e	Z = 1	1	2	*	*
JRNZ e	Z = 0	1	2	*	*
JRR b, rr, ee	Bit = 0	3	5	*	Δ
JRS b, rr, ee	Bit = 1	3	5	*	Δ

Notes:
b. 3-bit address
e. 5 bit signed displacement in the range -15 to +16
ee. 8 bit signed displacement in the range -126 to +129
rr. Data space register
Δ. Affected
*. Not Affected

Table 17. Bit Manipulation Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
SET b,rr	Bit Direct	2	4	*	*
RES b,rr	Bit Direct	2	4	*	*

Notes:
b. 3-bit address;
rr. Data space register;
*. Not Affected

Table 18. Control Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
NOP	Inherent	1	2	*	*
RET	Inherent	1	2	*	*
RETI	Inherent	1	2	Δ	Δ
STOP (1)	Inherent	1	2	*	*
WAIT	Inherent	1	2	*	*

Notes:
1. This instruction is deactivated and a WAIT is automatically executed instead of a STOP if the watchdog function is selected.
Δ. Affected
*. Not Affected

Table 19. Jump & Call Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
CALL abc	Extended	2	4	*	*
JP abc	Extended	2	4	*	*

Notes:
abc.12-bit address;
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Opcode Map Summary. The following table contains an opcode map for the instructions used by ST6

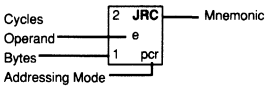
LOW / HI	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	LOW / HI
0 0000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b.d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 pcr	4 LD a,(y) 1 ind	0 0000
1 0001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b.d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 pcr	4 LD a,rr 2 dir	1 0001
2 0010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 CP a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b.d	2 JRZ e 1 pcr	4 COM a 1 inh	2 JRC e 1 pcr	4 CP a,(y) 1 ind	2 0010
3 0011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b.d.	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 pcr	4 CP a,rr 2 dir	3 0011
4 0100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 ADD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b.d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 pcr	4 ADD a,(y) 1 ind	4 0100
5 0101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b.d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 pcr	4 ADD a,rr 2 dir	5 0101
6 0110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 INC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b.d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 pcr	4 INC (y) 1 ind	6 0110
7 0111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b.d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 pcr	4 INC rr 2 dir	7 0111
8 1000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD (x),a 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b.d	2 JRZ e 1 pcr	# 	2 JRC e 1 pcr	4 LD (y),a 1 ind	8 1000
9 1001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC v 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b.d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 pcr	4 LD rr,a 2 dir	9 1001
A 1010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 AND a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b.d	2 JRZ e 1 pcr	4 RLC a 1 inh	2 JRC e 1 pcr	4 AND a,(y) 1 ind	A 1010
B 1011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b.d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 pcr	4 AND a,rr 2 dir	B 1011
C 1100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 SUB a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b.d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 pcr	4 SUB a,(y) 1 ind	C 1100
D 1101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b.d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 pcr	4 SUB a,rr 2 dir	D 1101
E 1110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 DEC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b.d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 pcr	4 DEC (y) 1 ind	E 1110
F 1111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b.d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 pcr	4 DEC rr 2 dir	F 1111

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

$Tj = T_A + PD \times RthJA$

Where : T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = $I_{DD} \times V_{DD}$ (chip internal power).

Pport = Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, V_{DD} = 4.5V	-5	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes :

- Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- (1) Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.

THERMAL CHARACTERISTIC

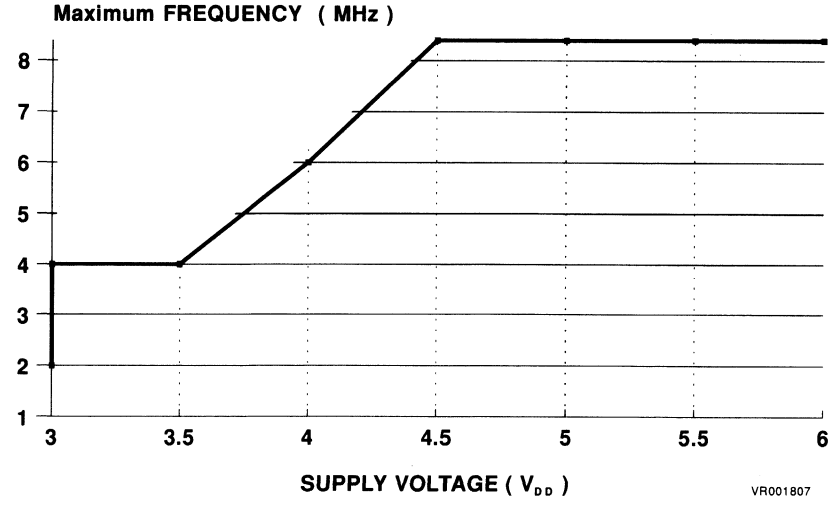
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28			55	°C/W
		PDIP20			60	
		PSO28			75	
		PSO20			80	

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	6 Suffix Version 1 Suffix Version	-40 0		85 70	°C
V_{DD}	Operating Supply Voltage	Low Voltage option f_{OSC}= 2MHz f_{INT} = 2MHz	2.5		6.0	V
		f_{OSC}= 4MHz f_{INT} = 4MHz	3.0		6.0	V
		f_{OSC} = 8MHz f_{INT} = 8MHz	4.5		6.0	V
f_{INT}	Internal Frequency (3)	V_{DD} = 3V V_{DD} = 4.5V	0 0		4.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input (1) Analog Inputs(2)	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input (1) Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

Notes :
1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (– 10%) can be expected to flow from the neighbouring pins.
2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.
3. An oscillator frequency above 1MHz is recommended for reliable A/D results.

Maximum Operating FREQUENCY (Fmax) Versus SUPPLY VOLTAGE (V_{DD})



The shaded area is outside the ST6260/65 operating range, device functionality is not guarenteed.

DC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage All inputs				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage All inputs		V_{DD} x 0.7			V
V_{Hys}	Hysteresis Voltage (4) All Inputs	V_{DD}=5V V_{DD}=3V	0.2 0.2			V
V_{OL}	Low Level Output Voltage Port A, C	V_{DD}=4.5V I_{OL} = +1.6mA V_{DD}=4.5V I_{OL} = +5.0mA V_{DD}=3.0V I_{OL} = +0.7mA			0.4 1.3 0.4	V
V_{OL}	Low Level Output Voltage Port B	V_{DD}=4.5V I_{OL} = +1.6mA V_{DD}=4.5V I_{OL}=+20.0mA V_{DD}=3.0V I_{OL} = +0.7mA			0.4 1.3 0.4	V
V_{OH}	High Level Output Voltage Port A, B, C	V_{DD}=4.5V I_{OL} = -1.6mA V_{DD}=4.5V I_{OL} = -5.0mA V_{DD}=3.0V I_{OL} = -0.7mA	4.1 3.5 2.6			V
I_{PU}	Input Pull-up Current Input Mode with Pull-up Port A, B, C, NMI	V_{IN} = V_{SS}, V_{DD}=2.5-6V			100	µA
I_{IL} I_{IH}	Input Leakage Current(1)	V_{IN} = V_{SS} V_{IN} = V_{DD}			1.0	µA
I_{DD}	Supply Current in RESET Mode	V_{RESET}=V_{SS} f_{OSC}=8MHz			3.5	mA
	Supply Current in RUN Mode (2)	V_{DD}=5.0V f_{INT}=8MHz V_{DD}=3.0V f_{INT}=4MHz			6.6 TBD	mA
	Supply Current in WAIT Mode (3)	V_{DD}=5.0V f_{INT}=8MHz V_{DD}=3.0V f_{INT}=4MHz			1.50 TBD	mA
	Supply Current in STOP Mode(3)	I_{LOAD}=0mA V_{DD}=5.0V			20	µA

Notes :
1. Only when pull-ups are not inserted
2. All peripherals running
3. EEPROM and A/D Converter in Stand-by
4. Hysteresis voltage between switching levels

AC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V V_{DD} = 4.5V			4 8	MHz
t_{OHL}	High to Low Transition Time	Port A, B, C C_L=100pF		40		ns
t_{OLH}	Low to High Transition Time	Port A, B, C C_L=100pF		40		
t_{SU}	Oscillator Start-up Time	C_{L1} = C_{L2} = 22pF V_{DD}x0.1 to V_{DD}x0.9		5	10	ms
t_{REC}	Supply Recovery Time (1)		100			
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin NMI pin		 100 100			ns
T_{WEE}	EEPROM Write Time	T_A = 25°C One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycle	Q_A L_{OT} Acceptance	300,000			cycles
Retention	EEPROM Data Retention	T_A = 25°C	10			years
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

Note:
1. Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.

I/O PORT CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins I_{OL}= 5mA , Standard I/O I_{OL}= 10mA , Port B I_{OL}= 20mA , Port B			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		0.1 0.1	1.0 1.0	µA
R_{PU}	Pull-up Resistor	Vin= 0V; All I/O Pins	50	100	200	KΩ

SPI CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{CL}	Clock Frequency at SCK				500	kHz
t_{SV}	Data Set up time on Sin			TBD		
t_H	Data hold time on Sin			TBD		
t_{TS}	Delay Transmission started on Sin	8MHz	0	Note 1		µs

Note 1. Minimum time 0µs
Maximum time 1 instruction cycle

TIMER1 CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIM1 Pin(1)				$\frac{f_{INT}}{4}$	MHz
t_W	Pulse Width at TIM1 Pin(1)	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	1 125 125			µs ns ns

Note:
1. Not available for ST6260

AR TIMER CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{1}{f_{INT}}$			s
f_{ARin}	Input Frequency on ARTIMin pin	STOP Mode RUN and WAIT Modes			2 $\frac{f_{INT}}{4}$	MHz MHz
t_W	Pulse Width at ARTIMin Pin	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	125 125 125			ns ns ns

A/D CONVERTER CHARACTERISTICS

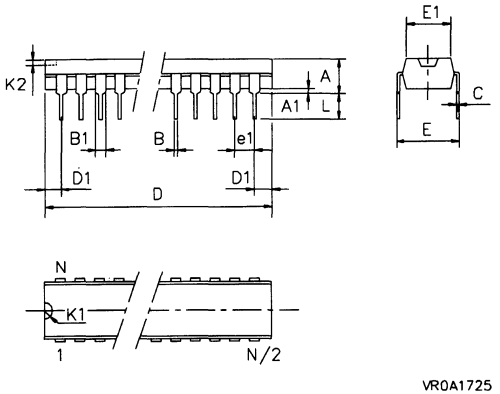
(T_A= -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution			8		Bit
A_{TOT}	Total Accuracy (1) (2)	f_{OSC} > 1.2MHz f_{OSC} > 32kHz			±2 ±4	LSB
tc	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when $V_{IN} = V_{SS}$	00			Hex
FSR	Full Scale Reading	Conversion result when $V_{IN} = V_{DD}$			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN}(3)	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance	Analog Channel switched just before conversion start (4)			30	kΩ

Notes:
1. Noise at V_{DD}, V_{SS} <10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

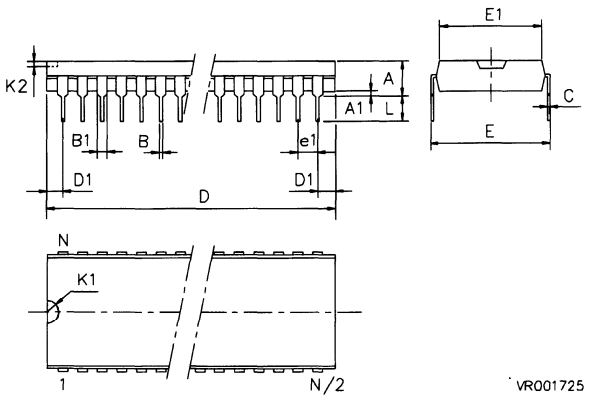
PACKAGE MECHANICAL DATA

Figure 54. 20-Pin Dual in Line Plastic (B), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.93			0.155
A1	0.254			0.010		
B			0.45			0.017
B1	1.39		1.65	0.055		0.065
C			0.25			0.009
D			25.4			1.000
D1			1.34			0.053
E		8.5			0.334	
E1			7.1			0.279
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L		3.30			0.129	
e1		2.54			0.10	
Number of Pins						
N	20					

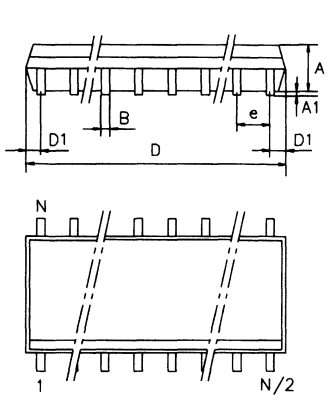
Figure 55. 28-Pin Dual in Line Plastic (B), 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		4.8	0.086		0.189
A1	0.51		1.77	0.010		0.069
B	0.38		0.58	0.015		0.023
B1	0.97		1.52	0.055		0.065
C	0.2		0.3	0.008		0.009
D	35.06		36.22	1.400		1.425
D1	–	–	–	–	–	–
E			16.3			0.641
E1		12.9				0.508
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	3.18		4.44	1.25		0.174
e1		2.54			0.10	
Number of Pins						
N	28					

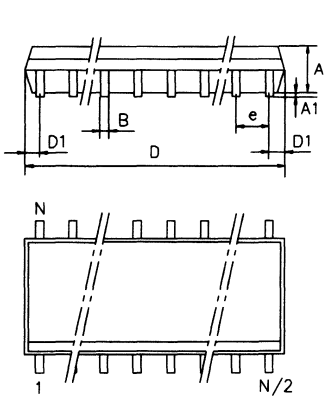
PACKAGES MECHANICAL DATA (Continued)

Figure 56. 20-Lead Small Outline Plastic (M), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	12.6		13.0	.4961		.5118
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	20					

Figure 57. 28-Lead Small Outline Plastic (M), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	17.7		18.1	.6969		.7125
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	28					

ORDERING INFORMATION

The following chapter deals with the procedure for transfer customer codes to SGS-THOMSON.

Communication of the customer code. Customer code is made up of the ROM contents and the list of the selected mask options. The ROM contents are to be sent on one diskette with the hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

The selected mask options are communicated to SGS-THOMSON using the correctly filled OPTION LIST appended.

Listing Generation & Verification. When SGS-THOMSON receives the diskette, a computer listing is generated from it. This listing refers exactly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. The signed listing constitutes a part of the contractual agreement for the creation of the customer mask.

SGS-THOMSON sales organization will provide detailed information on contractual points.

Table 20. ROM Memory Map

ST6260,ST6265 (4K ROM Devices)

Device Address	Description
0000h-007Fh	Reserved (1)
0080h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved (1)
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved (1)
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Notes :
1. Reserved Areas should be filled with FFh

ORDERING INFORMATION TABLE

Sales Type	ROM x8	I/O	Temperature Range	Package
ST6260B1/XXX ST6260B6/XXX	4K Bytes	13 13	0 to +70°C -40 to +85°C	PDIP20
ST6260M1/XXX ST6260M6/XXX	4K Bytes	13 13	0 to +70°C -40 to +85°C	PSO20
ST6265B1/XXX ST6265B6/XXX	4K Bytes	21 21	0 to +70°C -40 to +85°C	PDIP20
ST6265M1/XXX ST6265M6/XXX	4K Bytes	21 21	0 to +70°C -40 to +85°C	PSO20

Note: /XXX is a 2-3 alphanumeric character code added to the generic sales type on receipt of a ROM code and valid options.

ST6260, ST6265 MICROCONTROLLER OPTION LIST

Customer . . . . . .
Address . . . . . .
. . . . . .
Contact . . . . . .
Phone No . . . . . .
Reference . . . . . .

SGS-THOMSON Microelectronics references

Device:
[ ] ST6260, [ ] ST6265

Package:
[ ] Dual in Line Plastic
[ ] Small Outline Plastic
In this case, select conditioning
[ ] Standard (Stick)
[ ] Type 2 Reel

Temperature Range:
[ ] 0°C to + 70°C [ ] – 40°C to + 85°C

Special Marking:
[ ] No
[ ] Yes "_ _ _ _ _ _ _ _ _ _"
Authorized characters are letters, digits, '.', '–', '/' and spaces only.
Maximum character count are 10 char. for DIP packages and 8 char. for SO packages.

Watchdog Selection:
[ ] Hardware Activation (no STOP mode)
[ ] Software Activation (STOP mode available)

Power Supply:
[ ] Standard (3.0V to 6.0V)
For low Voltage (2.5V to 6.0V) Contact your Local SGS-THOMSON Office

Notes . . . . . .
. . . . . .
Signature . . . . . .

Date . . . . . .

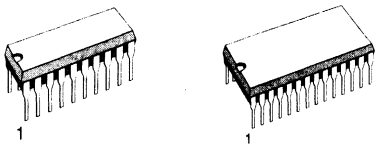
SGS-THOMSON MICROELECTRONICS

ST62E60, T60
ST62E65, T65

8-BIT EPROM HCMOS MCUs WITH A/D CONVERTER, EEPROM & AUTORELOAD TIMER

PRELIMINARY DATA

- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User EPROM: 3868 bytes
  Data ROM: User selectable size (in program EPROM)
  Data RAM: 128 bytes
  EEPROM: 128 bytes
- PDIP20, PSO20 (ST62T60) packages
- PDIP28, PSO28 (ST62T65) packages
- FDIP20W (ST62E60) packages
- FDIP28W (ST62E65) packages
- 13/21 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without Pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- 6/8 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer1)
- 8 bit Autoreload timer with 7-bit programmable prescaler (AR Timer)
- Digital Watchdog
- 8 bit A/D Converter with up to 7 (ST62E60,T60) and up to 13 (ST62E65,T65) analog inputs
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator (Quartz or Ceramic)
- Power-on Reset
- One external not maskable interrupt
- 9 powerful addressing modes

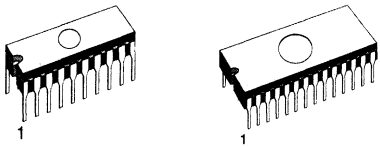


PDIP20 **PDIP28**

PSO20 **PSO28**

(Ordering Information at the end of the datasheet)

EPROM PACKAGES



FDIP20W **FDIP28W**

The ST62E60 and ST62E65 are the EPROM versions; ST62T60 and ST62T65 are the OTP versions; both are fully compatible with ST6260 and ST6265 ROM versions.

Figure 1. ST62E60/T60 Pin Configuration

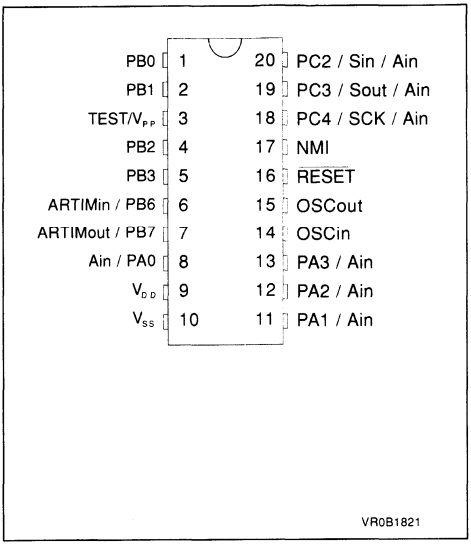


Figure 2. ST62E65/T65 Pin Configuration

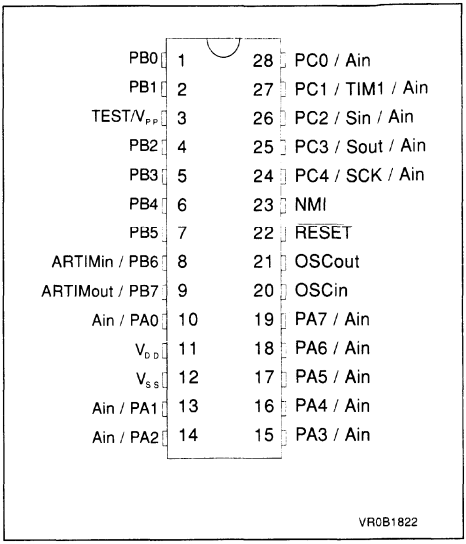
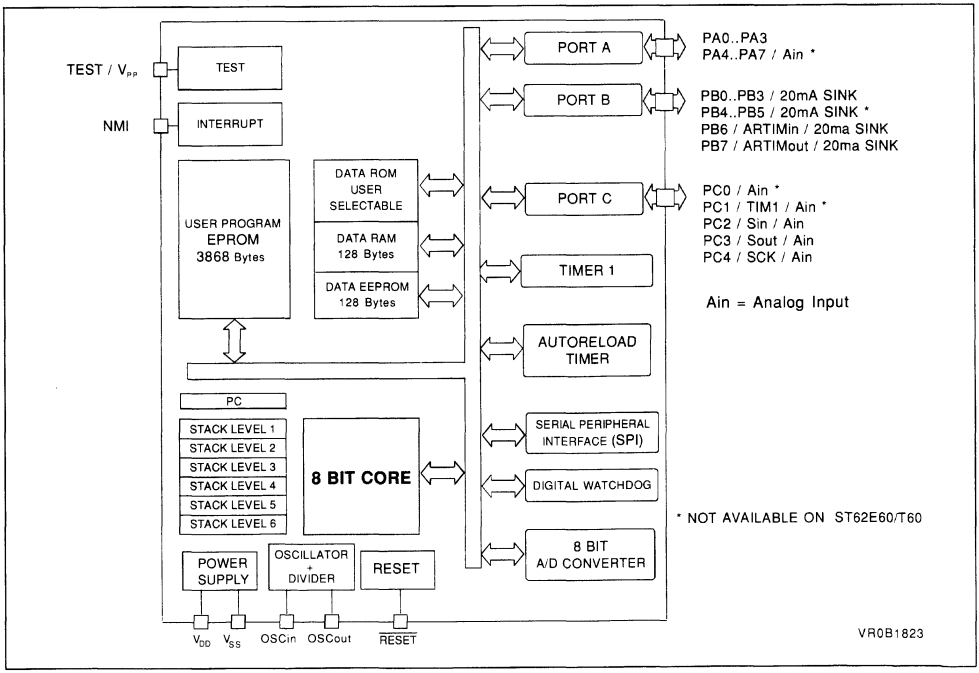


Figure 3. ST62E60,E65 Block Diagram



GENERAL DESCRIPTION

The ST62E60,T60,E65,T65 microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications.

They are the EPROM and OTP versions of the ST6260 and ST6265 devices. EPROM are suited for development. OTPs are suited for prototyping, preseries, low to mid volume series and inventory optimization for customer having several applications using the same MCU. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells).
The macrocells of the ST62E60, T60, E65 and T65 are: the timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer1), the 8-bit Auto-reload Timer with 7 bit programmable prescaler (AR Timer), the 8-bit A/D Converter with up to 7 (ST62E60,T60) and up to 13 (ST62E65,T65) analog inputs (A/D inputs are alternate functions of I/O pins), the Digital Watchdog (DWD) and an 8-bit Serial synchronous Peripheral Interface (SPI). In addition, these devices offer 128 bytes of EEPROM for non volatile data storage.
ST62E60 ,T60, E65 and T65 are well suited for automotive, appliance and industrial applications.

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The frequency at OSCin and OSCout is internally divided by 1, 2 or 4 by a software controlled divider.The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST. The TEST must be held at VSS for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous interrupt applying an external not maskable interrupt to the MCU. The NMI is falling edge sensitive. It is provided with an on-chip pull-up resistor and Schmitt trigger characteristics.

PC1/TIM1/Ain. This pin can be used as a Port C I/O bit, as Timer 1 I/O pin or as analog input for the on-chip A/D converter. This pin is available only on the ST62E65 and T65 (28 pin version). If programmed to be the Timer 1 pin, in input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time out occurs.
To use this pin as Timer 1 output a dedicated bit in the TIMER 1 Status/Control Register must be set. To use this pin as input pin the I/O pin has to be programmed as input. The analog mode should be programmed to use the line as an analog input.

PB6/ARTIMin, PB7/ARTIMout. These pins are either Port B I/O bits or the Input and Output pins of the Auto-reload Timer. To be used as timer input function PB6 has to be programmed as input with or without pull-up. A dedicated bit in the AR TIMER Mode Control Register sets PB7 as timer output function.

PA0-PA7. These 8 lines are organized as one I/O port (A). PA4-PA7 are not available on ST62E60 and T60 (20 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input, open-drain or push-pull output.

PB0-PB3, PB4, PB5. These 6 lines are organized as one I/O port (B). PB4, PB5 are available only on the ST62E65 and T65 (28 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED and TRIAC driving. The reset configuration of PB0-PB3 can be selected by mask option (pull-up or high impedance).

PC0-PC4. These 5 lines are organized as one I/O port (C). PC0 and PC1 are not available on ST62E60, T60 (20 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input for the A/D converter, open-drain or push-pull output. PC2-PC4 can also be used as respectively Data in, Data out and Clock I/O pins for the on-chip SPI to carry the synchronous serial I/O signals.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST6260,65 ROM DEVICE FOR FURTHER DETAILS.

EPROM/OTP DESCRIPTION

The ST62E60/E65 are the EPROM versions of the ST6260/65 products. They are intended for use during the development of an application and for pre-production and small volume production. ST62T60/T65 OTP have the same characteristics. They all include EPROM memory instead of the ROM memory of the corresponding ST6260/65, and so the program can be easily modified by the user with the ST62E6X EPROM programming tools from SGS-THOMSON.

From a user point of view (with the following exceptions) the ST62E60/E65 and ST62T60/T65 products have exactly the same software and hardware features as the ROM version. An additional mode is used to configure the part for programming of the EPROM, this is set by a +12.5V voltage applied to the TEST/V_{PP} pin. The programming of the ST62E60, T60, E65, T65 is described in the User Manual of the EPROM Programming Board.
Note also the Low Voltage option of ROM devices can not be emulated on EPROM or OTP devices

ROM Option Emulation

The ROM mask options that can be selected by the user in the ROM devices can be selected on the EPROM/OTP devices by an EPROM CODE byte that can be programmed with the ST62E6x EPROM programming tools available from SGS-THOMSON. This EPROM CODE byte is automatically read, and the selected options enabled, when the chip reset is activated.
The Option byte is written during programming either by using the PC menu (PC driven Mode) or automatically (stand-alone mode).

EPROM Programming Mode

An additional mode is used to configure the part for programming of the EPROM, this is set by a 12.5V voltage applied to the TEST/V_{PP} pin. The programming of the ST62E60/E65 and ST62T60/T65 is described in the User Manual of the EPROM Programming board.

EPROM ERASING

The EPROM of the windowed package of the ST62E60/E65 may be erased by exposure to Ultra Violet light.
The erasure characteristic of the ST62E60/E65 is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlights and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E60/E65 packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

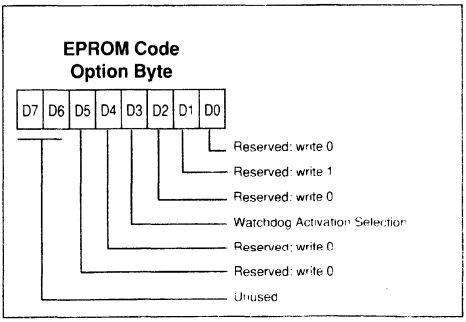
The recommended erasure procedure of the ST62E60/E65 EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537A. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E60/E65 should be placed within 2.5cm (1Inch) of the lamp tubes during erasure.

Table 1. ST62T60/T65 OTP Memory Map

Device Address	Description
0000h-007Fh	Reserved
0080h-0F9Fh	User Program ROM 3856 Bytes
0FA0h-0FEFh	Reserved
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved
0FFCh-0FFDh	NMI Vector
0FFEh-0FFFh	User Reset Vector

Note. Reserved Areas should be filled with FFh

Figure 4. EPROM Code Option Byte



D7-D6. These bits are not used.

D5-D4. Must be cleared to zero.

D3. This bit selects the on-chip Watchdog activation. If cleared to zero this bit selects the software activation, if set to one, it selects the hardware activation option.

D2-D0. Must be cleared to zero.

D1. Must be set to one.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

$T_j = T_A + PD \times RthJA$

Where : T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = $I_{DD} \times V_{DD}$ (chip internal power).

Pport = Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, VDD = 4.5V	-5	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes :

- Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- (1) Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28			55	°C/W
		PDIP20			60	
		PSO28			75	
		PSO20			80	

RECOMMENDED OPERATING CONDITIONS

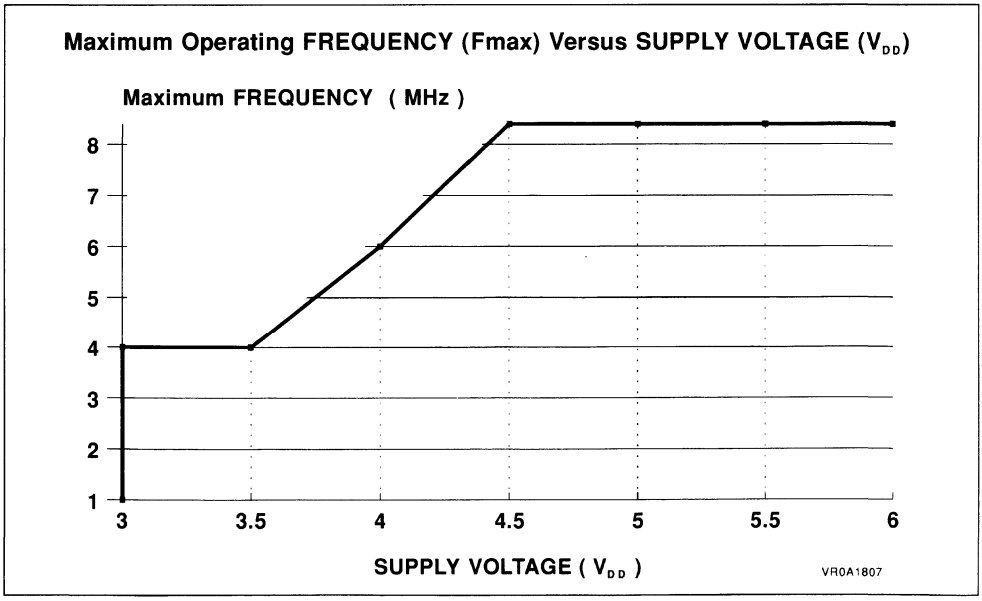
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	6 Suffix Version 1 Suffix Version	-40 0		85 70	°C
V_{DD}	Operating Supply Voltage	f_{OSC}= 4MHz f_{INT} = 4MHz	3.0		6.0	V
		f_{OSC} = 8MHz f_{INT} = 8MHz	4.5		6.0	V
f_{INT}	Internal Frequency (3)	V_{DD} = 3V V_{DD} = 4.5V	0 0		4.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input (1) Analog Inputs(2)	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input (1) Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

Notes :

1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (– 10%) can be expected to flow from the neighbouring pins.

2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.

3. An oscillator frequency above 1MHz is recommended for reliable A/D results.



The shaded area is outside the device operating range, device functionality is not guarenteed.

DC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage All inputs				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage All inputs		V_{DD} x 0.7			V
V_{Hys}	Hysteresis Voltage (4) All Inputs	V_{DD}=5V V_{DD}=3V	0.2 0.2			V
V_{OL}	Low Level Output Voltage Port A, C	V_{DD}=4.5V I_{OL} = +1.6mA V_{DD}=4.5V I_{OL} = +5.0mA V_{DD}=3.0V I_{OL} = +0.7mA			0.4 1.3 0.4	V
V_{OL}	Low Level Output Voltage Port B	V_{DD}=4.5V I_{OL} = +1.6mA V_{DD}=4.5V I_{OL}=+20.0mA V_{DD}=3.0V I_{OL} = +0.7mA			0.4 1.3 0.4	V
V_{OH}	High Level Output Voltage Port A, B, C	V_{DD}=4.5V I_{OL} = -1.6mA V_{DD}=4.5V I_{OL} = -5.0mA V_{DD}=3.0V I_{OL} = -0.7mA	4.1 3.5 2.6			V
I_{PU}	Input Pull-up Current Input Mode with Pull-up Port A, B, C, NMI	V_{IN} = V_{SS}, V_{DD}=3-6V			100	µA
I_{IL} I_{IH}	Input Leakage Current(1)	V_{IN} = V_{SS} V_{IN} = V_{DD}			1.0	µA
I_{DD}	Supply Current in RESET Mode	V_{RESET}=V_{SS} f_{OSC}=8MHz			3.5	mA
	Supply Current in RUN Mode (2)	V_{DD}=5.0V f_{INT}=8MHz V_{DD}=3.0V f_{INT}=4MHz			6.6 TBD	mA
	Supply Current in WAIT Mode (3)	V_{DD}=5.0V f_{INT}=8MHz V_{DD}=3.0V f_{INT}=4MHz			1.50 TBD	mA
	Supply Current in STOP Mode(3)	I_{LOAD}=0mA V_{DD}=5.0V			20	µA

Notes :

1.Only when pull-ups are not inserted
2.All peripherals running
3.EEPROM and A/D Converter in Stand-by
4.Hysteresis voltage between switching levels

AC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V V_{DD} = 4.5V			4 8	MHz
t_{OHL}	High to Low Transition Time	Port A, B, C C_L=100pF		40		ns
t_{OLH}	Low to High Transition Time	Port A, B, C C_L=100pF		40		
t_{SU}	Oscillator Start-up Time	C_{L1} = C_{L2} = 22pF V_{DD}x0.1 to V_{DD}x0.9		5	10	ms
t_{REC}	Supply Recovery Time (1)		100			
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin NMI pin		 100 100			ns
T_{WEE}	EEPROM Write Time	T_A = 25°C One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycle	Q_A L_{OT} Acceptance	300,000			cycles
Retention	EEPROM Data Retention	T_A = 25°C	10			years
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

Note:

1. Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.

I/O PORT CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins I_{OL}= 5mA , Standard I/O I_{OL}= 10mA , Port B I_{OL}= 20mA , Port B			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		0.1 0.1	1.0 1.0	µA
R_{PU}	Pull-up Resistor	Vin= 0V; All I/O Pins	50	100	200	KΩ

SPI CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{CL}	Clock Frequency at SCK				500	kHz
t_{SV}	Data Set up time on Sin			TBD		
t_H	Data hold time on Sin			TBD		
t_{TS}	Delay Transmission started on Sin	8MHz	0	Note 1		µs

Note :

1. Minimum time 0µs
   Maximum time 1 instruction cycle

TIMER1 CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIM1 Pin(1)				$\frac{f_{INT}}{4}$	MHz
t_W	Pulse Width at TIM1 Pin(1)	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	1 125 125			µs ns ns

Note:

1.Not available for ST6260

AR TIMER CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{1}{f_{INT}}$			s
f_{ARin}	Input Frequency on ARTIMin pin	STOP Mode RUN and WAIT Modes			2 $\frac{f_{INT}}{4}$	MHz MHz
t_W	Pulse Width at ARTIMin Pin	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	125 125 125			ns ns ns

A/D CONVERTER CHARACTERISTICS

(T_A= -40 to +85°C unless otherwise specified)

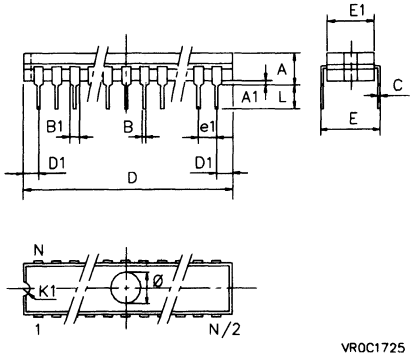
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution (1)			8		Bit
A_{TOT}	Total Accuracy (1)	f_{OSC} > 1.2MHz f_{OSC} > 32kHz			±2 ±4	LSB
t_C (2)	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when Vin = V_{SS}	00			Hex
FSR	Full Scale Reading	Conversion result when Vin = V_{DD}			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN} (3)	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance				30	KΩ
SSI	Analog Reference Supply Impedence				2	KΩ

Notes:

1. Noise at V_{DD}, V_{SS} <10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

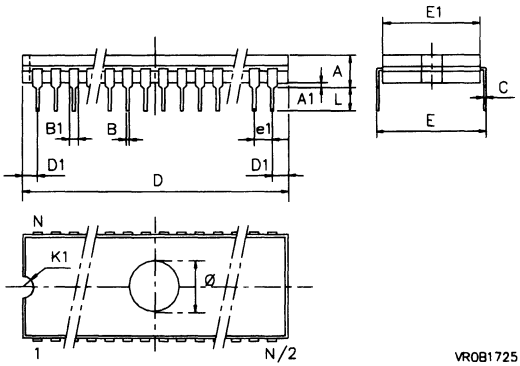
PACKAGE MECHANICAL DATA

20-Lead Frit Seal Ceramic Dual in Line Package, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.27		1.52	0.050		0.060
C	0.22		0.31	0.009		0.012
D			26.92			1.059
D1	0.51		1.27	0.020		0.050
E	–	–	–	–	–	–
E1			7.80			0.307
L	3.40			0.134		
e1	2.29		2.79	0.090		0.110
Ø	4.24		4.39	0.167		0.173
	Number of Pins					
N	20					

28-Lead Frit Seal Ceramic Dual in Line Package, 600-Mil Widht



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.17		1.42	.046		.056
C	0.22		0.31	0.009		0.012
D			38.10			1.500
D1	1.52		2.49	.060		.098
E	–	–	–	–	–	–
E1	13.05		13.36	.514		.526
L	3.00			.118		
e1	2.29		2.79	0.090		0.110
Ø	6.86		7.36	.270		.290
	Number of Pins					
N	28					

ORDERING INFORMATION

Please contact your local SGS-THOMSON marketing contact for ordering information

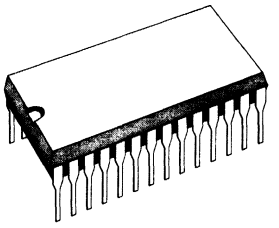
SGS-THOMSON MICROELECTRONICS

ST6294

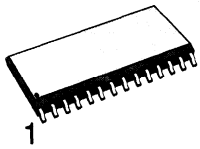
8-BIT HCMOS MCU WITH A/D CONVERTER, EEPROM & AUTO-RELOAD TIMER

PRELIMINARY DATA

- 3 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -25 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User ROM: 3868 bytes
- Data ROM: User selectable size (in program ROM)
- Data RAM: 128 bytes
- EEPROM: 128 bytes
- PDIP28, PSO28 packages
- 21 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- 8 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer1)
- 8 bit auto-reload timer with 7-bit programmable prescaler (AR Timer)
- Digital Watchdog
- 8 bit A/D Converter with up to 13 analog inputs
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator (Quartz Crystal or Ceramic)
- Power-on Reset
- Clock output
- 9 powerful addressing modes
- The development tool of the ST6294 microcontrollers consists of the ST626x-EMU emulation and development system connected via a standard RS232 serial line to an MS-DOS Personal Computer



PDIP28



PSO28

(Ordering Information at the end of the datasheet)

Figure 1. ST6294 Pin Configuration

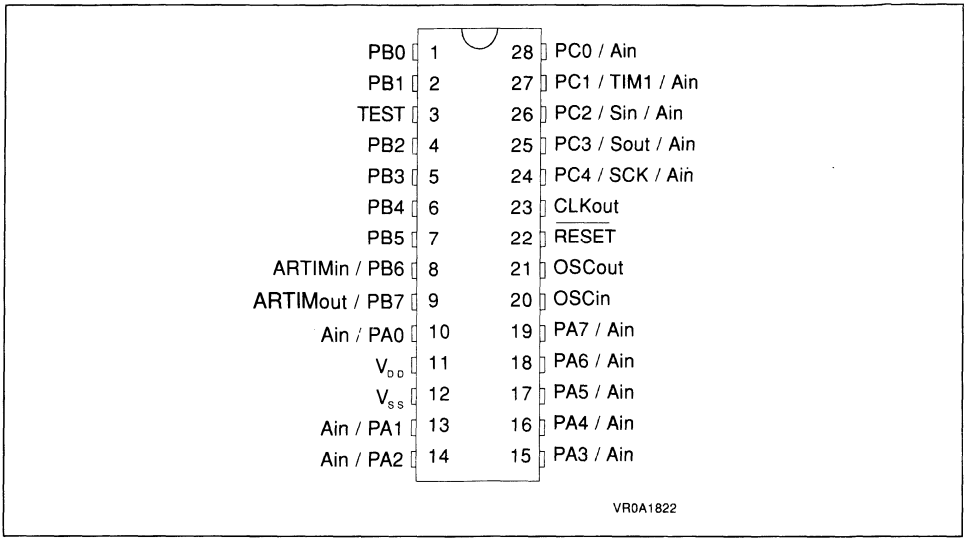
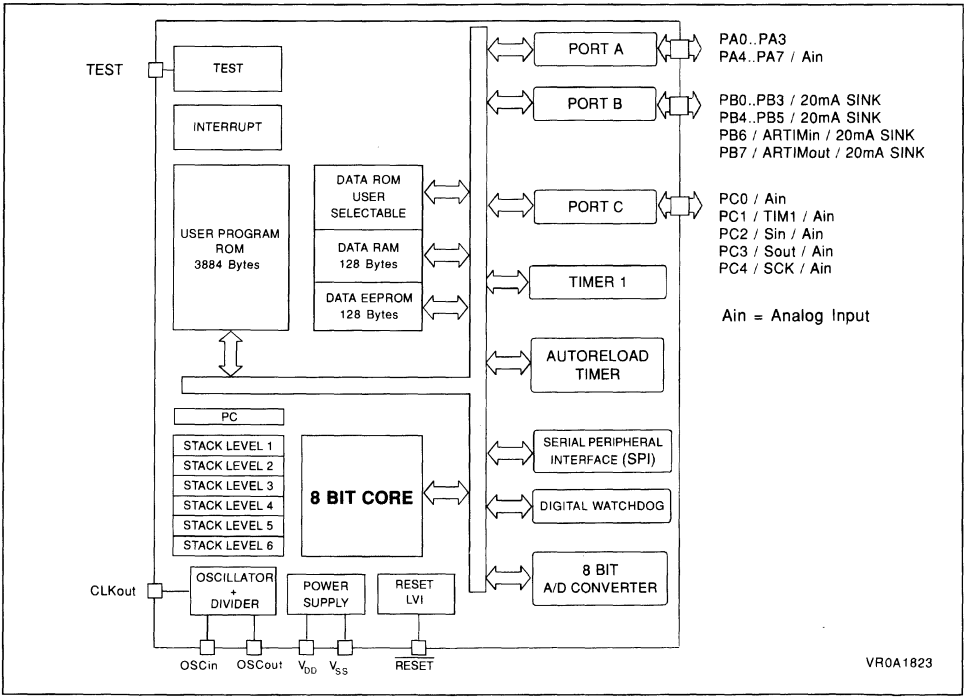


Figure 2. ST6294 Block Diagram



GENERAL DESCRIPTION

The ST6294 microcontroller is member of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells).

The macrocells of the ST6294 are: the Timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer1), the 8-bit Auto-reload Timer with 7 bit programmable prescaler (AR Timer), the 8-bit A/D Converter with up to 13 analog inputs (A/D inputs are alternate functions of I/O pins), the Digital Watchdog (DWD) and an 8-bit Serial synchronous Peripheral Interface (SPI). In addition, these devices offer 128 bytes of EEPROM for non volatile data storage.
The ST6294 is a version of the ST6265 specifically tailored to be used in telephone set applications. The only difference is that a CKOUT pin is provided instead of the NMI pin. *For this reason this datasheet only contains information relating to the differences to the ST6265, and thus should be read in conjunction with the ST6265 datasheet.* The ST62E94 EPROM version is available for prototypes and low-volume production; also OTP version is available.

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The frequency at OSCin and OSCout is internally divided by 1, 2 or 4 by a software controlled divider.The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST. The TEST must be held at V_{SS} for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

CKOUT. This clock pin outputs the oscillator frequency divided by 2 ($f_{OSC}/2$). This function can be disabled by software to reduce power consumption.

PC1/TIM1/Ain. This pin can be used as a Port C I/O bit, as Timer 1 I/O pin or as analog input for the on-chip A/D converter. If programmed to be the Timer 1 pin, in input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time out occurs.
To use this pin as Timer 1 output a dedicated bit in the TIMER 1 Status/Control Register must be set. To use this pin as input pin the I/O pin has to be programmed as input. The analog mode should be programmed to use the line as an analog input.

PB6/ARTIMin, PB7/ARTIMout. These pins are either Port B I/O bits or the Input and Output pins of the Auto-reload Timer. To be used as timer input function PB6 has to be programmed as input with or without pull-up. A dedicated bit in the AR TIMER Mode Control Register sets PB7 as timer output function.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input, open-drain or push-pull output.

PB0-PB3, PB4, PB5. These 6 lines are organized as one I/O port (B). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED and TRIAC driving. The reset configuration of PB0-PB3 can be selected by mask option (pull-up or high impedance).

PC0-PC4. These 5 lines are organized as one I/O port (C). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input for the A/D converter, open-drain or push-pull output. PC2-PC4 can also be used as respectively Data in, Data out and Clock I/O pins for the on-chip SPI to carry the synchronous serial I/O signals.

ST6294 DESCRIPTION

The ST6294 is a version of the ST6265 standard device dedicated to telephone set application.

From a user point of view (with the following exceptions) the ST6294 product has exactly the same software and hardware features as the ST6265.

NMI

There is no external NMI pin in the ST6294. Although the ST6294 uses the standard ST62 core, which includes the NMI function. The user program therefore cannot place the ST62 in NMI mode. However, NMI mode is the default mode at power on or after a system reset generated by the watchdog or through the RESET pin. In these cases, the user software must perform a RETI instruction to exit from NMI mode to enable further interrupts from other sources prior to any other instruction. The ST6265 data sheet must therefore be read in this respect.

CKOUT PIN

The CKOUT pin is a dedicated output pin which enables a stabilized clock output to drive external circuits without any additional components. The clock output can be disabled by software to reduce power cosumption.

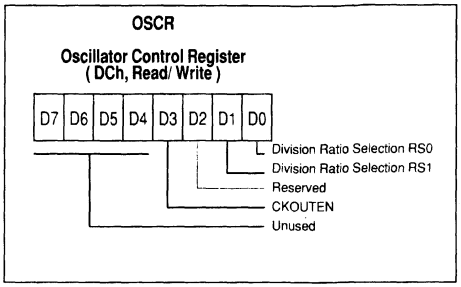
The output frequency is the oscillator frequency (before the Oscillator Divider) divided by 2 ($f_{OSC}/2$). The CKOUT pin is enabled through bit CKOUTEN of the Oscillator Control Register, at address DCh. The CKOUT pin provides high drive current capability.

Note :

When enabled through the CKOUTEN bit, the clock output increases the device overall power consumption by around 200µA. It should therefore be disabled when the lowest power consumption is required.

Oscillator Control Register

Figure 3. Oscillator Control Register



D7-D4. These bits are not used.

CKOUTEN. This bit, when cleared to zero, enables the output of the oscillator frequency divided by 2 at pin CKOUT. When it is set to one, pin CKOUT is held high. CKOUTEN is cleared on reset.

D2. Reserved. Must be kept low.

RS1-RS0. These bits select the division ratio of the Oscillator Divider in order to generate the internal frequency. The following selections are available:

RS1	RS0	Division Ratio
0	0	1
0	1	2
1	0	4
1	1	4

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

$Tj = T_A + PD \times RthJA$

Where : T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = $I_{DD} \times V_{DD}$ (chip internal power).

Pport = Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, V_{DD} = 4.5V	-5	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes :

- Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- (1) Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28			55	°C/W
		PSO28			75	

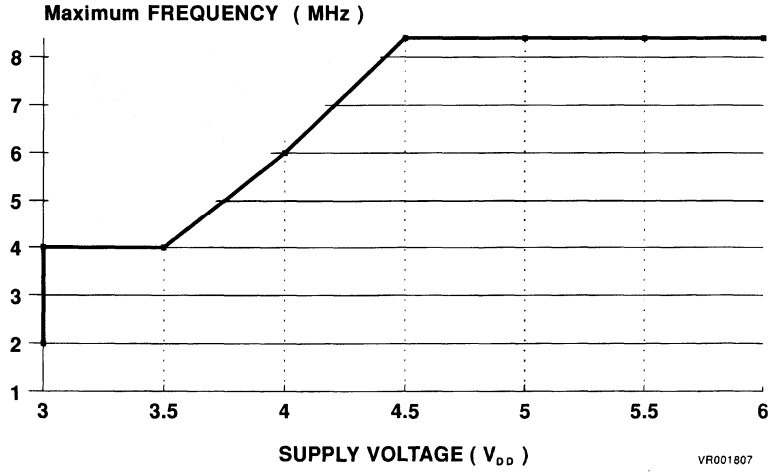
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	8 Suffix Version	-25		85	°C
V_{DD}	Operating Supply Voltage	f_{OSC}= 4MHz f_{INT} = 4MHz	3.0		6.0	V
		f_{OSC} = 8MHz f_{INT} = 8MHz	4.5		6.0	V
f_{INT}	Internal Frequency (3)	V_{DD} = 3V V_{DD} = 4.5V	0 0		4.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input (1) Analog Inputs (2)	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input (1) Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

Notes :

1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (~ 10%) can be expected to flow from the neighbouring pins.
2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.
3. An oscillator frequency above 1MHz is recommended for reliable A/D results.

Maximum Operating FREQUENCY (Fmax) Versus SUPPLY VOLTAGE (V_{DD})



The shaded area is outside the ST6294 operating range, device functionality is not guaranteed.

DC ELECTRICAL CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage All inputs				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage All inputs		V_{DD} x 0.7			V
V_{OL}	Low Level Output Voltage	V_{DD}=5V I_{OL} = 10µA, All I/O pins CKOUT I_{OL} = 5mA, Standard I/O CKOUT I_{OL} = 10mA, Port B I_{OL} = 20mA, Port B			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	V_{DD}=5V I_{OH} = -10µA I_{OH} = -5.0mA I_{OH} = -1.5mA, V_{DD}=3V	4.9 3.5 2.0			V
I_{PU}	Input Pull-up Current Input Mode with Pull-up Port A, B, C,	V_{IN} = V_{SS}, V_{DD}=3.0-6V			100	µA
I_{IL} I_{IH}	Input Leakage Current(1)	V_{IN} = V_{SS} V_{IN} = V_{DD}			1.0	µA
I_{DD}	Supply Current in RESET Mode	V_{RESET}=V_{SS},f_{OSC}=4MHz V_{DD}<3.8V V_{DD}<6.0V			0.70 1.25	mA
	Supply Current in RUN Mode (2)	V_{DD}=6.0V, f_{INT}=8MHz All peripherals on (1)			6.6	mA
		V_{DD}=3.8V, f_{INT}=4MHz All peripherals on (1)			1.5	mA
		V_{DD}=3.8V, f_{INT}=1MHz f_{OSC}=4MHz Peripherals disabled (2)			0.65	mA
	Supply Current in WAIT Mode (3)	V_{DD}=6.0V, f_{INT}=8MHz Peripherals disabled (3) V_{DD}=3.8V, f_{INT}=4MHz Peripherals disabled (3)			1.30 0.35	mA
	Supply Current in STOP Mode	V_{DD}=6.0V			20	µA

Notes :

1. A/D Converter running, EEPROM enabled; Timer 1 and AR Timer running; CKOUTpin enabled. When the EEPROM is in write cycle, an additional 300µA must be added to I_{DD}max
2. A/D Converter in Stand-by; EEPROM in Stand-by; CKOUT pin disabled
3. A/D Converter in Stand-by; EEPROM in Stand-by; CKOUT pin disabled; Timer 1 and AR Timer stopped
4. Hysteresis voltage between switching levels

AC ELECTRICAL CHARACTERISTICS

(T_A = -25to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V V_{DD} = 4.5V			4 8	MHz
t_{OHL}	High to Low Transition Time	Port A, B, C, CKOUT C_L=100pF		40		ns
t_{OLH}	Low to High Transition Time	Port A, B, C, CKOUT C_L=100pF		40		
t_{SU}	Oscillator Start-up Time	C_{L1} = C_{L2} = 22pF V_{DD}=5V		5	10	ms
t_{REC}	Supply Recovery Time (1)		100			
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin, NMI pin		100			ns
T_{WEE}	EEPROM Write Time	T_A = 25°C One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycle	Q_A L_{OT} Acceptance	300.000			cycles
Retention	EEPROM Data Retention	T_A = 25°C	10			years
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

Note:

1. Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.

I/O PORT CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins, CKOUT I_{OL}= 5mA , Standard I/O, CKOUT I_{OL}= 10mA , Port B I_{OL}= 20mA , Port B			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		0.1 0.1	1.0 1.0	µA

SPI CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{CL}	Clock Frequency at SCK				500	kHz
t_{SV}	Data Set up time on Sin			TBD		
t_H	Data hold time on Sin			TBD		
t_{TS}	Delay Transmission started on Sin	8MHz	0	Note 1		µs

Note 1. Minimum time: 0µs
Maximum time: 1 instruction cycle

TIMER1 CHARACTERISTICS
(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIM1 Pin				$\frac{f_{INT}}{8}$	MHz
t_W	Pulse Width at TIM1 Pin	V_{DD} = 3.0V $V_{DD} \geq$ 4.5V	1 125			µs ns

AR TIMER CHARACTERISTICS
(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{1}{f_{INT}}$			s
f_{ARin}	Input Frequency on ARTIMin pin	STOP Mode RUN and WAIT Modes			2 $\frac{f_{INT}}{4}$	MHz MHz
t_W	Pulse Width at ARTIMin Pin	V_{DD} = 3.0V $V_{DD} \geq$ 4.5V	125 125			ns ns

A/D CONVERTER CHARACTERISTICS

(T_A= -25 to +85°C unless otherwise specified)

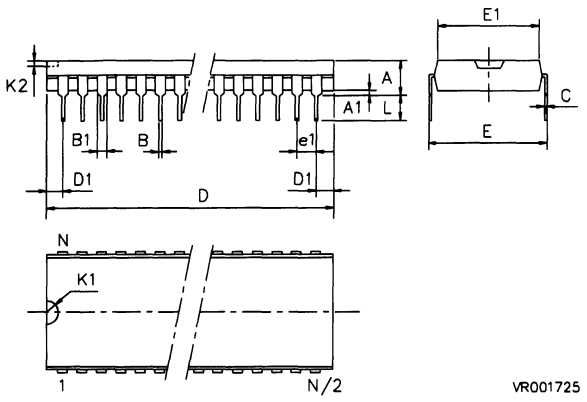
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution			8		Bit
A_{TOT}	Total Accuracy (1) (2)	f_{OSC} > 1.2MHz f_{OSC} > 32kHz			±2 ±4	LSB
t_C	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when $V_{IN} = V_{SS}$	00			Hex
FSR	Full Scale Reading	Conversion result when $V_{IN} = V_{DD}$			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN} (3)	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance	Analog Channel switched just before conversion start (4)			30	kΩ

Notes:

1. Noise at V_{DD}, V_{SS} <10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

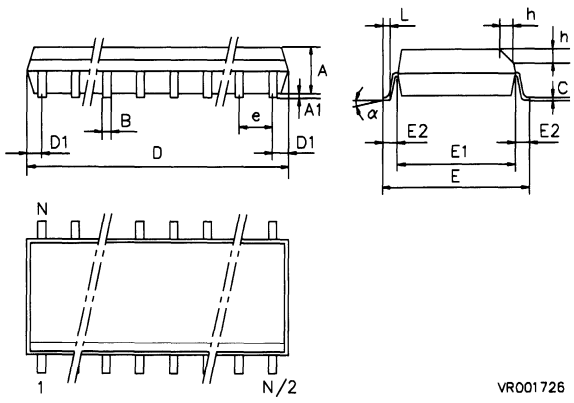
PACKAGE MECHANICAL DATA

Figure 4. 28-Pin Dual in Line Plastic (B), 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		4.8	0.086		0.189
A1	0.51		1.77	0.010		0.069
B	0.38		0.58	0.015		0.023
B1	0.97		1.52	0.055		0.065
C	0.2		0.3	0.008		0.009
D	35.06		36.22	1.400		1.425
D1	–	–	–	–	–	–
E			16.3			0.641
E1		12.9				0.508
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	3.18		4.44	1.25		0.174
e1		2.54			0.10	
Number of Pins						
N	28					

Figure 5. 28-Lead Small Outline Plastic (M), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	17.7		18.1	.6969		.7125
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	28					

ORDERING INFORMATION

The following chapter deals with the procedure for transfer customer codes to SGS-THOMSON.

Communication of the customer code. Customer code is made up of the ROM contents and the list of the selected mask options. The ROM contents are to be sent on one diskette with the hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

The selected mask options are communicated to SGS-THOMSON using the correctly filled OPTION LIST appended.

Listing Generation & Verification. When SGS-THOMSON receives the diskette, a computer listing is generated from it. This listing refers exactly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. The signed listing constitutes a part of the contractual agreement for the creation of the customer mask.

SGS-THOMSON sales organization will provide detailed information on contractual points.

Table 1. ROM Memory Map

ST6294 (4K ROM Devices)

Device Address	Description
0000h-007Fh	Reserved (1)
0080h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved (1)
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved (1)
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Note 1. Reserved Areas should be filled with FFh

ORDERING INFORMATION TABLE

Sales Type	ROM x8	I/O	Temperature Range	Package
ST6294B8/XXX	4K Bytes	21	-25 to + 85°C	PDIP28
ST6294M8/XXX	4K Bytes	21	-25 to +85°C	PSO28

Note: /XXX is a 2-3 alphanumeric character code added to the generic sales type on receipt of a ROM code and valid options.

ST6294 MICROCONTROLLER OPTION LIST

Customer .....

Address .....

.....

Contact .....

Phone No .....

Reference .....

SGS-THOMSON Microelectronics references

Device:
[ ] ST6294

Package: [ ] Dual in Line Plastic [ ] Small Outline Plastic

In this case, select conditioning

[ ] Standard (Stick)
[ ] Tape & Reel

Temperature Range: [ ] -25°C to + 85°C

Special Marking: [ ] No

[ ] Yes "_ _ _ _ _ _ _ _ _ _ _ _"

Authorized characters are letters, digits, '.', '–', '/' and spaces only.
Maximum character count is 10 char. for DIP packages
and 8 char. for SO packages.

PB0/PB1 Status during reset

[ ] Input with pull-up [ ] High impedance

PB2/PB3 Status during reset

[ ] Input with pull-up [ ] High impedance

Watchdog Selection:

[ ] Hardware Activation (no STOP mode) [ ] Software Activation (STOP mode available)

Notes .....

.....

Signature .....

Date .....

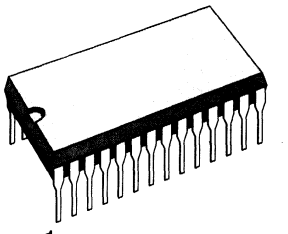
SGS-THOMSON MICROELECTRONICS

ST62E94, T94

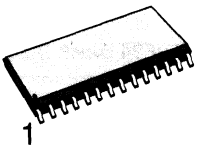
8-BIT EPROM HCMOS MCUs WITH A/D CONVERTER, EEPROM & AUTORELOAD TIMER

PRELIMINARY DATA

- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -25 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User EPROM: 3868 bytes
  Data ROM: User selectable size (in program EPROM)
  Data RAM: 128 bytes
  EEPROM: 128 bytes
- PDIP28, PSO28 (ST62T94) packages
- CDIP28W (ST62E94) packages
- 21 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without Pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- 8 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer1)
- 8 bit Autoreload timer with 7-bit programmable prescaler (AR Timer)
- Digital Watchdog
- 8 bit A/D Converter with up to analog inputs
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator (Quartz or Ceramic)
- Power-on Reset
- Clock output
- 9 powerful addressing modes



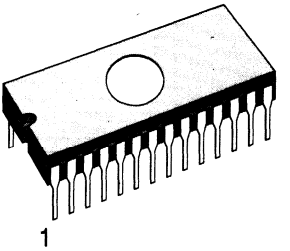
PDIP28



PSO28

(Ordering Information at the end of the datasheet)

EPROM PACKAGES



CDIP28W

The ST62E94 is the EPROM version; ST62T94 is the OTP version; both are fully compatible with ST6294 ROM version.

Figure 1. ST62E94/T94 Pin Configuration

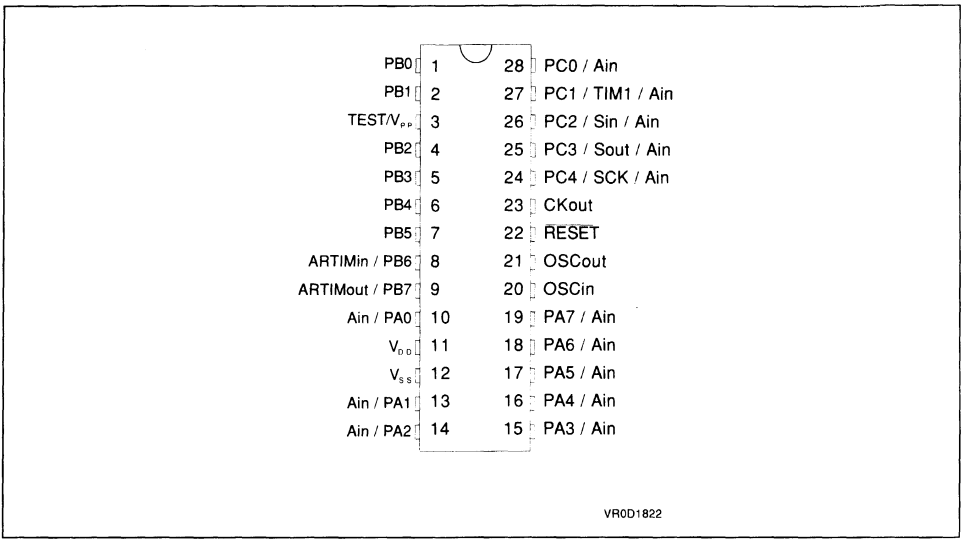
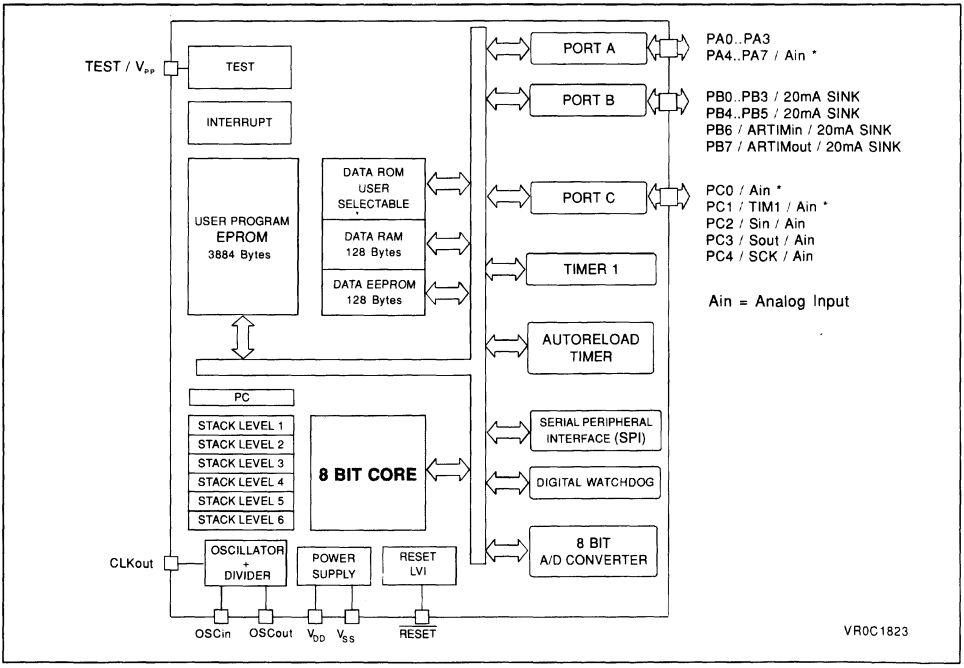


Figure 2. ST62E94 Block Diagram



GENERAL DESCRIPTION

The ST62E94,T94 microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications.

They are the EPROM and OTP versions of the ST6294 device. EPROM are suited for development. OTPs are suited for prototyping, preseries, low to mid volume series and inventory optimization for customer having several applications using the same MCU. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells).
The macrocells of the ST62E94, T94 are: the timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer1), the 8-bit Auto-reload Timer with 7 bit programmable prescaler (AR Timer), the 8-bit A/D Converter with up to 13 analog inputs (A/D inputs are alternate functions of I/O pins), the Digital Watchdog (DWD) and an 8-bit Serial synchronous Peripheral Interface (SPI). In addition, these devices offer 128 bytes of EEPROM for non volatile data storage.
The ST62E94 ,T94 are a version of the ST62E65, T65 specifically tailored to be used in telephone set applications. The only difference is that a CKOUT pin is provided instead of the NMI input pin.

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The frequency at OSCin and OSCout is internally divided by 1, 2 or 4 by a software controlled divider.The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST. The TEST must be held at VSS for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

CKOUT. This clock pin outputs the oscillator frequency divided by 2 ($f_{OSC}/2$). This function can be disabled by software to reduce power consumption.

PC1/TIM1/Ain. This pin can be used as a Port C I/O bit, as Timer 1 I/O pin or as analog input for the on-chip A/D converter. If programmed to be the Timer 1 pin, in input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time out occurs.
To use this pin as Timer 1 output a dedicated bit in the TIMER 1 Status/Control Register must be set. To use this pin as input pin the I/O pin has to be programmed as input. The analog mode should be programmed to use the line as an analog input.

PB6/ARTIMin, PB7/ARTIMout. These pins are either Port B I/O bits or the Input and Output pins of the Auto-reload Timer. To be used as timer input function PB6 has to be programmed as input with or without pull-up. A dedicated bit in the AR TIMER Mode Control Register sets PB7 as timer output function.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input, open-drain or push-pull output.

PB0-PB3, PB4, PB5. These 6 lines are organized as one I/O port (B). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED and TRIAC driving.

PC0-PC4. These 5 lines are organized as one I/O port (C). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input for the A/D converter, open-drain or push-pull output. PC2-PC4 can also be used as respectively Data in, Data out and Clock I/O pins for the on-chip SPI to carry the synchronous serial I/O signals.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST6294 DEVICE FOR FURTHER DETAILS.

EPROM/OTP DESCRIPTION

The ST62E94 is the EPROM version of the ST6294 product. It is intended for use during the development of an application and for pre-production and small volume production. ST62T94 OTP has the same characteristics. It includes EPROM memory instead of the ROM memory and so the program can be easily modified by the user with the ST62E6x EPROM programming tools from SGS-THOMSON.

From a user point of view (with the following exceptions) the ST62E94, T94 products have exactly the same software and hardware features as the ROM version. An additional mode is used to configure the part for programming of the EPROM, this is set by a +12.5V voltage applied to the TEST/V_{PP} pin. The programming of the ST62E94, T94 is described in the User Manual of the EPROM Programming Board.
Note also the Low Voltage option of ROM devices can not be emulated on EPROM or OTP devices

ROM Option Emulation

The ROM mask options that can be selected by the user in the ROM devices can be selected on the EPROM/OTP devices by an EPROM CODE byte that can be programmed with the ST62E6x EPROM programming tools available from SGS-THOMSON. This EPROM CODE byte is automatically read, and the selected options enabled, when the chip reset is activated.
The Option byte is written during programming either by using the PC menu (PC driven Mode) or automatically (stand-alone mode).

EPROM Programming Mode

An additional mode is used to configure the part for programming of the EPROM, this is set by a 12.5V voltage applied to the TEST/V_{PP} pin. The programming of the ST62E94, T94 is described in the User Manual of the EPROM Programming board.

EPROM ERASING

The EPROM of the windowed package of the ST62E94 may be erased by exposure to Ultra Violet light.
The erasure characteristic of the ST62E94 is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlights and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E94 packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

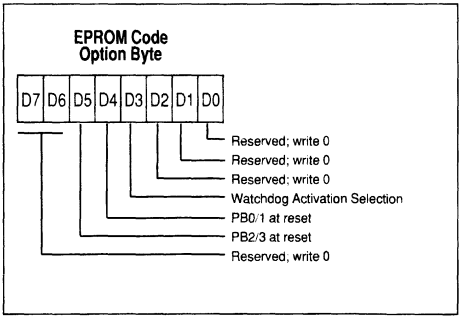
The recommended erasure procedure of the ST62E94 EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537A. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E94 should be placed within 2.5cm (1Inch) of the lamp tubes during erasure.

Table 1. ST62E94/T94 OTP Memory Map

Device Address	Description
0000h-007Fh	Reserved
0080h-0F9Fh	User Program ROM 3856 Bytes
0FA0h-0FEFh	Reserved
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved
0FFCh-0FFDh	NMI Vector
0FFEh-0FFFh	User Reset Vector

Note. Reserved Areas should be filled with FFh

Figure 3. EPROM Code Option Byte



D7-D6. These bits are not used.

D5. This bit selects the configuration of the ports PB2 and PB3 during reset. If set to zero, PB2 and PB3 are configured with pull-up during reset. If set to one, PB2 and PB3 are configured as high impedance ports.

D4. Same as D5 for PB0 and PB1.

D3. This bit selects the on-chip Watchdog activation. If cleared to zero this bit selects the software activation, if set to one, it selects the hardware activation option.

D2-D0. Must be cleared to zero.

D1. Must be set to zero.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

$Tj = T_A + PD \times RthJA$

Where : T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = $I_{DD} \times V_{DD}$ (chip internal power).

Pport = Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3 (1)	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3 (1)	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, VDD = 4.5V	-5	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes :

- Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- (1) Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.

THERMAL CHARACTERISTIC

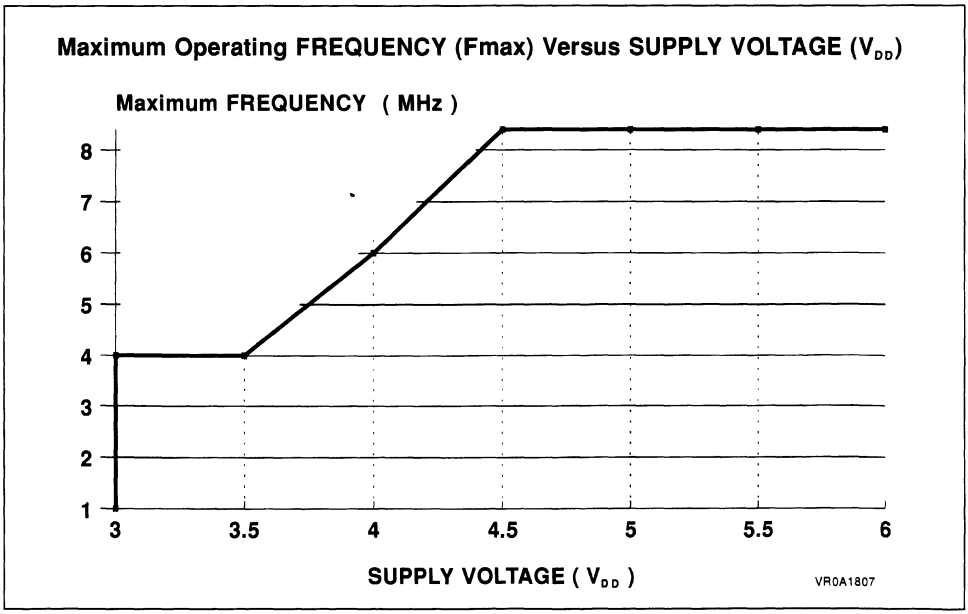
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28			55	°C/W
		PSO28			75	

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	8 Suffix Version 1 Suffix Version	-25 0		85 70	°C
V_{DD}	Operating Supply Voltage	f_{OSC}= 4MHz f_{INT} = 4MHz f_{OSC} = 8MHz f_{INT} = 8MHz	3.0 4.5		6.0 6.0	V V
f_{INT}	Internal Frequency (3)	V_{DD} = 3V V_{DD} = 4.5V	0 0		4.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input (1) Analog Inputs(2)	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input (1) Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

Notes :

1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (~ 10%) can be expected to flow from the neighbouring pins.
2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.
3. An oscillator frequency above 1MHz is recommended for reliable A/D results.



The shaded area is outside the device operating range, device functionality is not guaranteed.

DC ELECTRICAL CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage All inputs				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage All inputs		V_{DD} x 0.7			V
V_{OL}	Low Level Output Voltage	V_{DD}=5V I_{OL} = 10µA, All I/O pins CKOUT I_{OL} = 5.0mA, Standard I/O CKOUT I_{OL} = 10mA, Port B I_{OL} = 20mA, Port B			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	V_{DD}=5V I_{OH} = -10µA I_{OH}= -5.0mA I_{OH} = -1.5mA, V_{DD}=3V	4.9 3.5 2.0			V
I_{PU}	Input Pull-up Current Input Mode with Pull-up Port A, B, C	V_{IN} = V_{SS}, V_{DD}=3.0-6V			100	µA
I_{IL} I_{IH}	Input Leakage Current(1)	V_{IN} = V_{SS} V_{IN} = V_{DD}			1.0	µA
I_{DD}	Supply Current in RESET Mode	V_{RESET}=V_{SS},f_{OSC}=4MHz V_{DD}<3.8V V_{DD}<6.0V			0.70 1.25	mA
	Supply Current in RUN Mode (2)	V_{DD}=6.0V, f_{INT}=8MHz All peripherals on (1)			6.6	mA
		V_{DD}=3.8V, f_{INT}=4MHz All peripherals on (1)			1.50	mA
		V_{DD}=3.8V, f_{INT}=1MHz f_{OSC}=4MHz Peripherals disabled (2)			0.65	mA
	Supply Current in WAIT Mode (3)	V_{DD}=6.0V, f_{INT}=8MHz Peripherals disabled (3) V_{DD}=3.8V, f_{INT}=4MHz Peripherals disabled (3)			1.30 0.35	mA
	Supply Current in STOP Mode	V_{DD}=6.0V			20	µA

Notes :

1. A/D Converter running, EEPROM enabled; Timer 1 and AR Timer running; CKOUTpin enabled. When the EEPROM is in write cycle, an additional 300µA must be added to IDDmax
2. A/D Converter in Stand-by; EEPROM in Stand-by; CKOUT pin disabled
3. A/D Converter in Stand-by; EEPROM in Stand-by; CKOUT pin disabled; Timer 1 and AR Timer stopped
4. Hysteresis voltage between switching levels

AC ELECTRICAL CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V V_{DD} = 4.5V			4 8	MHz
t_{OHL}	High to Low Transition Time	Port A, B, C, CKOUT C_L=100pF		40		ns
t_{OLH}	Low to High Transition Time	Port A, B, C, CKOUT C_L=100pF		40		
t_{SU}	Oscillator Start-up Time	C_{L1} = C_{L2} = 22pF V_{DD}=5V		5	10	ms
t_{REC}	Supply Recovery Time (1)		100			
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin, NMI pin		100 100			ns
T_{WEE}	EEPROM Write Time	T_A = 25°C One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycle	Q_A L_{OT} Acceptance	300,000			cycles
Retention	EEPROM Data Retention	T_A = 25°C	10			years
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

Note:

1. Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.

I/O PORT CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins, CKOUT I_{OL}= 5mA , Standard I/O, CKOUT I_{OL}= 10mA , Port B I_{OL}= 20mA , Port B			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		0.1 0.1	1.0 1.0	µA
R_{PU}	Pull-up Resistor	Vin= 0V; All I/O Pins	50	100	200	KΩ

SPI CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{CL}	Clock Frequency at SCK				500	kHz
t_{SV}	Data Set up time on Sin			TBD		
t_H	Data hold time on Sin			TBD		
t_{TS}	Delay Transmission started on Sin	8MHz	0	Note 1		µs

Note :

1. Minimum time: 0µs
   Maximum time: 1 instruction cycle

TIMER1 CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIM1 Pin				$\frac{f_{INT}}{8}$	MHz
tw	Pulse Width at TIM1 Pin	V_{DD} = 3.0V $V_{DD} \geq$ 4.5V	1 125			µs ns

AR TIMER CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{1}{f_{INT}}$			s
f_{ARin}	Input Frequency on ARTIMin pin	STOP Mode RUN and WAIT Modes			2 $\frac{f_{INT}}{4}$	MHz MHz
tw	Pulse Width at ARTIMin Pin	V_{DD} = 3.0V $V_{DD} \geq$4.5V	125 125			ns ns

A/D CONVERTER CHARACTERISTICS

(T_A= -25 to +85°C unless otherwise specified)

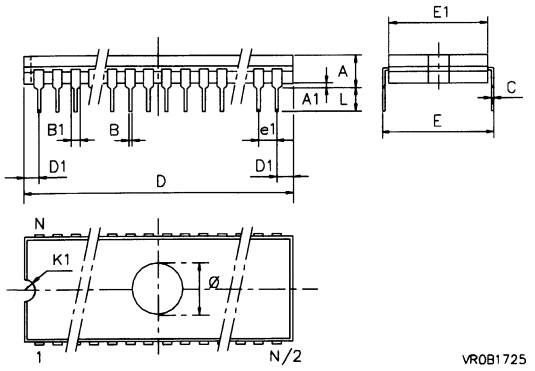
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution (1)			8		Bit
A_{TOT}	Total Accuracy (1)	f_{OSC} > 1.2MHz f_{OSC} > 32kHz			±2 ±4	LSB
t_C (2)	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when Vin = V_{SS}	00			Hex
FSR	Full Scale Reading	Conversion result when Vin = V_{DD}			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN} (3)	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance				30	KΩ
SSI	Analog Reference Supply Impedence				2	KΩ

Notes:

1. Noise at VDD, VSS <10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

PACKAGE MECHANICAL DATA

Figure 4. 28-Lead Frit Seal Ceramic Dual in Line Package, 600-Mil Widht



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.17		1.42	.046		.056
C	0.22		0.31	0.009		0.012
D			38.10			1.500
D1	1.52		2.49	.060		.098
E	–	–	–	–	–	–
E1	13.05		13.36	.514		.526
L	3.00			.118		
e1	2.29		2.79	0.090		0.110
Ø	6.86		7.36	.270		.290
	Number of Pins					
N	28					

ORDERING INFORMATION

ORDERING INFORMATION TABLE

Sales Type	OTP/EPROM	I/O	Additional Features	Temperature Range	Package
ST62T94B8	OTP 4K Bytes	21	CKOUT Pin	-25° to + 85°C	PDIP28
ST62T94M8					PSO28
ST62E94F1	EPROM 4K Bytes	21	CKOUT Pin	0 to + 70°C	CDIP28

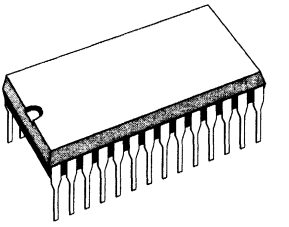
SGS-THOMSON MICROELECTRONICS

ST7291

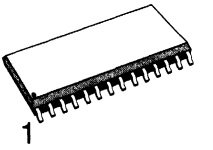
8-BIT HCMOS MCUs WITH 16K ROM AND WAKE-UP FUNCTION

PRELIMINARY DATA

- 3 to 5.5V supply operating range
- 8MHz Maximum Clock Frequency
- Fully static operation
- 0 to +70°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention Modes
- User ROM: 16K bytes
- Data RAM: 256 bytes
- 28 pin Dual In Line and SO plastic packages
- 19 bidirectional I/O lines
- 8 lines programmable as interrupt wake-up inputs
- 16-bit timer with one output compare (without output pin).
- Interrupt Wake-up function
- Low voltage detector
- Master Reset and power on reset
- Full Hardware Emulator
- 8-bit data manipulation
- 74 basic instructions
- 10 main addressing modes
- 8x8 unsigned multiply instruction
- True bit manipulation
- Complete development support on real time emulator with PC/DOS
- Full software package (Cross Assembler, debugger)



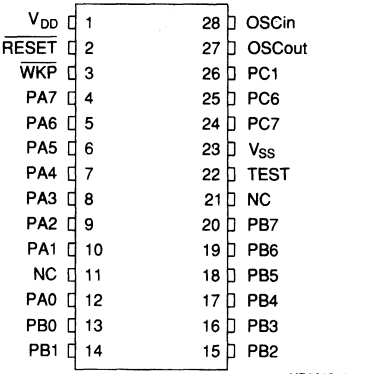
PDIP28



PSO28

(Ordering Information at the end of the datasheet)

PIN DESCRIPTION

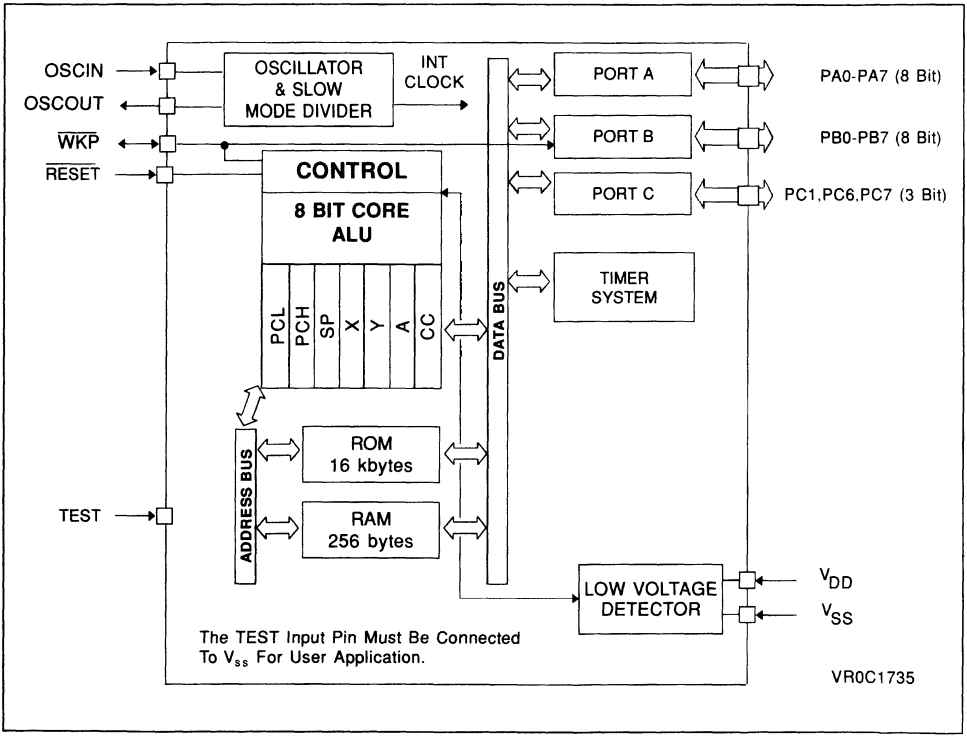


1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST7291 is a HCMOS microcontroller unit (MCU) from the ST72 family. It is based around an industry standard 8 bit core and offers an enhanced instruction set. The processor runs with an external clock at 8 MHz with a 5V supply and 4MHz with a 3.3V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST7291 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST7291 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes an on-chip oscillator, CPU, ROM, RAM, I/O, one timer with one output compare system, and a low voltage detector.

Figure 1. ST7291 Block Diagram



1.2 PIN DESCRIPTION

V_{DD}. Single power supply voltage 3 to 5.5 volts.

V_{SS}. Ground

OSCin, OSCout. Oscillator input and output pins. These pins are to be connected to a parallel resonant crystal or ceramic resonator. An external clock source can also be input through OSCin.

$\overline{RESET}$. The active low input signal forces the initialization of the MCU. This event is the first priority interrupt.

$\overline{WKP}$ is the external, software maskable interruptsignal. This I/O pin may be connected to the PORT B through 30kΩ resistor, enabling the wake-up function of PORT B.

PA0-PA7, PB0-PB7, PC1, PC6, PC7. These 19 lines are standard I/O lines, programmable as either input or output.

- PORT A 8 Standard I/O lines accessed through DDRA and DRA Registers. .
- PORT B. 8 Standard I/O lines accessed through DDRB and DRB Registers. According to the state of the WFD control bit, the 8 PORT B bits are 8 Standard I/O port or pull-up bits, with a wake-up interrupt function.
- PORT C. 3 Standard I/O lines accessed through DDRC and DRC Registers (PC1, PC6 and PC7).

TEST. Input test pin. In the user mode, this pin must be connected to V_{SS}.

Table 1. ST7291 Pin Configuration

Name	Function	Description	Pin Assignment
V_{DD}	I	Power supply	1
$\overline{RESET}$	I	RESET	2
$\overline{INT}$	I/O	Wake-up Interrupt Signal	3
PA7	I/O	Standard Port	4
PA6	I/O	Standard Port	5
PA5	I/O	Standard Port	6
PA4	I/O	Standard Port	7
PA3	I/O	Standard Port	8
PA2	I/O	Standard Port	9
PA1	I/O	Standard Port	10
NC			11
PA0	I/O	Standard Port	12
PB0	I/O	Standard Port (with Wake-up Interrupt Signal)	13
PB1	I/O	Standard Port (with Wake-up Interrupt Signal)	14
PB2	I/O	Standard Port (with Wake-up Interrupt Signal)	15
PB3	I/O	Standard Port (with Wake-up Interrupt Signal)	16
PB4	I/O	Standard Port (with Wake-up Interrupt Signal)	17
PB5	I/O	Standard Port (with Wake-up Interrupt Signal)	18
PB6	I/O	Standard Port (with Wake-up Interrupt Signal)	19
PB7	I/O	Standard Port (with Wake-up Interrupt Signal)	20
NC			21
TEST	I	Test Input	22
V_{SS}	I	Ground	23
PC7	I/O	Standard Port	24
PC6	I/O	Standard Port	25
PC1	I/O	Standard Port	26
OSCout	O	Oscillator	27
OSCin	I	Oscillator	28

1.3 CENTRAL PROCESSING UNIT

1.3.1 Introduction

The CPU has a full 8-bit architecture. Six internal registers allow efficient 8-bit data manipulations. The CPU is able to execute 74 basic instructions. It features 10 main addressing modes. It is able to address 16384 bytes of memory and registers with its program counter.

1.3.2 CPU Registers

The 6 CPU registers are shown in the programming model in Figure 2. Following an interrupt, the registers are pushed onto the stack in the order shown in Figure 3. They are popped from stack in the reverse order. The Y register is not affected by these automatic procedures. The interrupt routine must therefore handle it, if needed, through the POP and PUSH instructions.

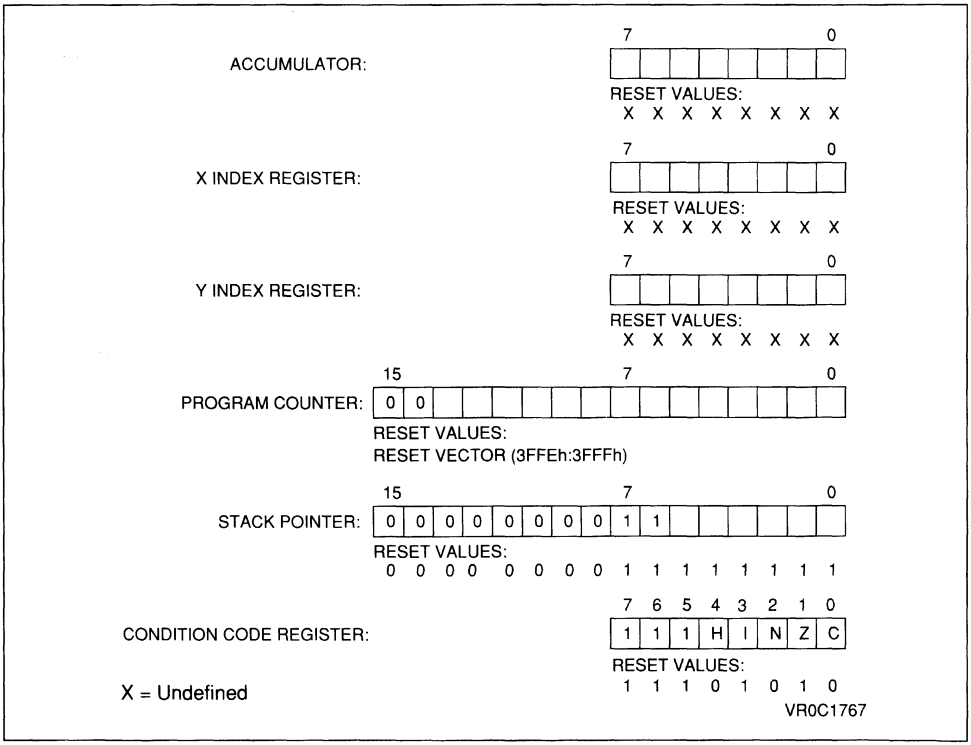
Accumulator (A). The accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations as well as data manipulations.

Index Registers (X and Y). These 8-bit registers are used to create effective addresses or as temporary storage area for data manipulations. The cross assembler generates a PRECEDE instruction (PRE) to indicate that the following instruction refers to the Y register. The Y register is never automatically stacked. Interrupt routines must push or pop it by using the POP and PUSH instructions.

Program Counter (PC). The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. In the ST7291, only the 14 low order bits are used, bits 14 and 15 are forced to "0".

Stack Pointer (SP). The stack pointer is a 16-bit register. The 6 least significant bits contain the address of the next free location of the stack. The 10 most significant bits are forced as indicated in Figure 2. They are reserved for future extension of ST72 family.

Figure 2. Programming Model



CENTRAL PROCESSING UNIT (Continued)

The stack is used to save the CPU context on subroutines calls or interrupts. The user can also directly use it through the POP and PUSH instructions.

After a MCU reset or after the reset stack pointer instruction (RSP), the stack pointer is set to its upper value (0FFh). It is then decremented after data has been pushed onto the stack and incremented after data is popped from the stack. When the lower limit is exceeded, the stack pointer wraps around to the stack upper limit. The previously stored information is then over written and therefore lost.

A subroutine call occupies two locations and an interrupt five locations.

1.3.3 Condition Code Register (CC).

The condition code register is a 5 bit register which indicates the result of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. The following paragraphs describe each bit.

Half carry bit (H). The H bit is set to 1 when a carry occurs between the bits 3 and 4 of the ALU during an ADD or ADC instruction. The H bit is useful in BCD arithmetic subroutines.

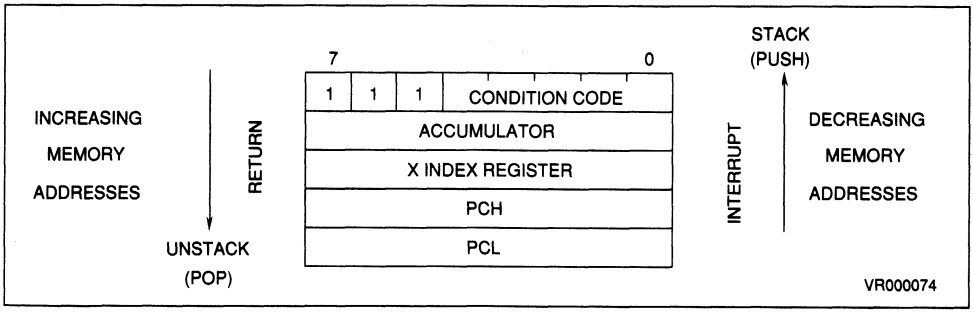
Interrupt mask (I). When the I bit is set to 1, all interrupts are disabled. Clearing this bit enables them. Interrupts requested while I is set are latched and can be processed when I is cleared (only one interrupt request per interrupt enable flag can be latched).

Negative (N). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is negative (i.e. the most significant bit is a logic 1).

Zero (Z). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

Carry/Borrow (C). When set, C indicates that a carry or borrow out of the ALU occurred during the last arithmetic operation. This bit is also affected during bit test, branch, shift and rotate instructions.

Figure 3. Stacking Order



1.4 MEMORY MAP

As shown in Figure 4, the MCU is capable of addressing 16384 bytes of memory and I/O registers. In the ST7291, 16144 of these bytes are user accessible.

The locations consist of 32 bytes of I/O registers, 256 bytes of RAM and 15840 Kbytes of user ROM. The RAM space includes 64 bytes for the stack from 00C0h to 00FFh. Programs that only use a small part of the allocated stack locations for interrupts and/or subroutine stacking purpose can use the remaining bytes as standard RAM locations.

The highest address bytes contains the user defined reset and interrupt vectors.

Figure 4. Memory Map

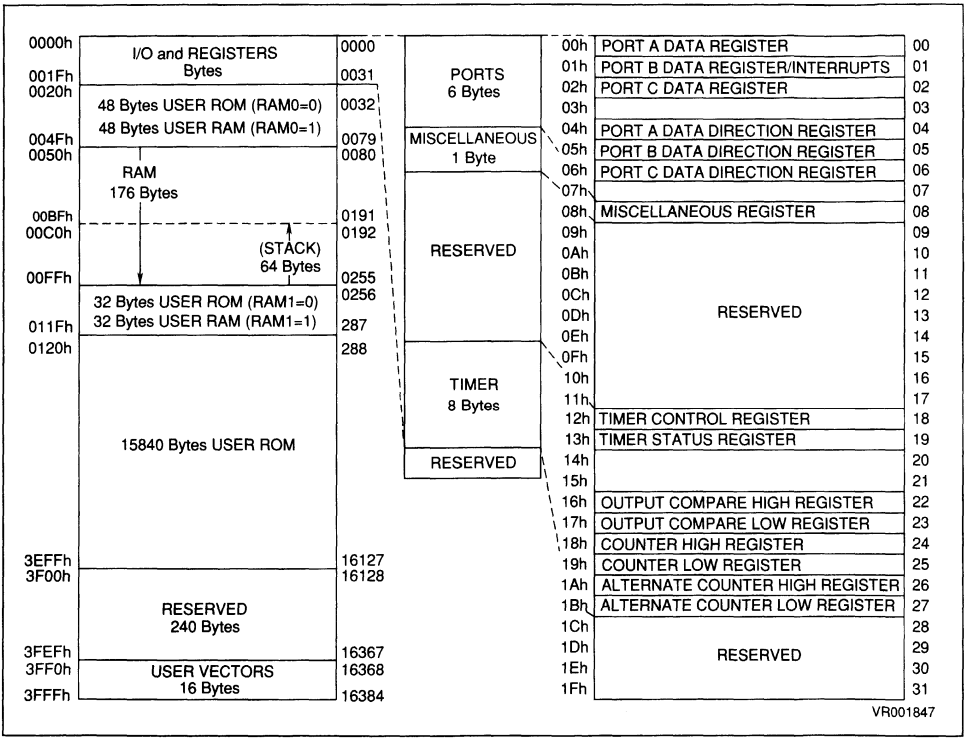


Table 2. Interrupt Vectors

Register	Source	Interrupts	CPU Interrupt	Vector Address
N/A	N/A	RESET	RESET	3FFEh, 3FFFh
N/A	N/A	SOFTWARE	TRAP	3FFCh, 3FFDh
N/A	WKP (pin 3)	PORT B	EXT. INT.	3FFAh, 3FFBh
TIMER STATUS	OCF/TOF	TIMER	TIMER	3FF8h, 3FF9h
MISCELLANEOUS	LVDF	LVD	LVD	3FF6h, 3FF7h
N/A	N/A	N/A	N/A	3FF4h, 3FF5h
N/A	N/A	N/A	N/A	3FF2h, 3FF3h
N/A	N/A	N/A	N/A	3FF0h, 3FF1h

1.5 LOW VOLTAGE DETECTOR

The low voltage detector circuitry forces to one level the flag LVDF in the MISCELLANEOUS Register and generates an interrupt request if the bit LVDIE in the MISCELLANEOUS Register is high when the power supply falls below 3.5V (Typical case).

The flag LVDF and the interrupt request are directely the result of the low voltage detector and they are not resettable by software condition. As long as the power supply remains lower than 3.5 volts the flag is forced to one level and the interrupt request is activated by the detector (if LVDIE=1).

The low voltage detector has a static power consumption less than 0.1 mA typical for a 5 volts power supply. It can be disabled putting the LVDON control bit in the MISCELLANEOUS Register to low level; in this case the flag LVDF is forced to zero and the detector is disabled in order to eliminate the static consumption.

The starting time of the LVD is lower than 5µs. It means that the flag LVDF is undetermined during 5µs after putting the bit LVDON to high.

Low Voltage Detector During low power modes

The HALT instruction disables the low voltage detector in order to suppress any static current.

The flag LVDF is forced to zero during the HALT mode.

If the micro is waked up by the key board interrupt, the starting address of the subroutine program will be 3FFAh-3FFBh even if the interrupt request of the LVD is activated. if the user wants to have a higher priority for the interrupt request of the LVD he can do that putting a RIM (Reset Interrupt Mask) instruction at the beginning of the key board subroutine. In this case the program counter will jump to the starting address 3FF6h-3FF7h just after the RIM instruction to execute the LVD subroutine instead of the wake-up subroutine. At the end of the LVD subroutine the software will continue to execute the wake-up subroutine.

The wait instruction has no effect on the low voltage detector.

1.6 MISCELLANEOUS REGISTER (08h)

Read/Write

Reset Value: 0000 0010 (02h)

7							0
RAM0	RAM1	0	LVDIE	LVDON	LVDF	INT	WFD

Bit 7 = **RAM0** *Random Access Memory Control Bit 0*
RAM0 = 0 Maps 48 Bytes of ROM into page zero from 0020h to 004Fh.
RAM0 = 1 Maps 48 Bytes of RAM into page zero from 0020h to 004Fh.

Bit 6 = **RAM1** *Random Access Memory Control Bit 1*
RAM1 = 0 Maps 32 Bytes of ROM into page one from 0100h to 011Fh.
RAM1 = 1 Maps 32 Bytes of RAM into page one from 0100h to 011Fh.

Bit 5 = Unused

Bit 4 = **LVDIE** *Low Voltage Interrupt Enable*
LVDIE = 0 Disables the Interrupt Request of the LVD.
LVDIE = 1 Enables the Interrupt Request of the LVD.

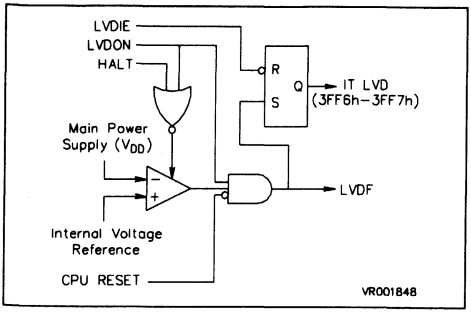
Bit 3 = **LVDON** *Low Voltage Detector Enable*
LVDON = 0 Disables the Low Voltage Detector (no static power consumption). LVDF is forced to low level.
LVDON = 1 Enables the Low Voltage Detector.

Bit 2 = **LVDF** *Low Voltage Detector Flag*
LVDF is set by the LVD when the main power supply (V_{DD}) is lower than 3.5V if the LVDON control bit is high. This flag is always forced to low when the bit LVDON is written to 0.

Bit 1 = **INT** *Interrupt Request*
INT = 0 Selects the edge only option.
INT = 1 Selects the edge and level option.
The INT bit can only be written once after RESET.

Bit 0 = **WFD** *Wake-up Feature Disable*
WFD = 0 Enables the Wake-up function on Port B.
WFD = 1 Disables the Wake-up function on Port B. All resistors of the Port B are disconnected from the WKP pad.

Figure 5. Block Diagram



1.7 CLOCK SYSTEM

General Description

The MCU accepts either a Crystal/Ceramic resonator or an external clock to provide the internal oscillator. The internal clock (fop) is derived by a divide-by-2 from the external oscillator frequency (f_{OSC}).

Crystal . The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for fosc. The circuit shown on Figure 7 is recommended when using a crystal. The table lists the recommended capacitance and feedback resistance values.

Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and startup stabilization time.

Ceramic Resonator. A ceramic resonator may be used in place of the crystal in low cost applications. The circuit on Figure 7 is recommended when using a ceramic resonator. The table lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

External Clock. An external clock should be applied to the OSCin input with the OSCout pin not connected, as shown on Figure 8. The t_{OXOV} and t_{ILCH} specifications do not apply when using an external clock input. The equivalent specification of the external clock source should be used instead of t_{OXOV} or t_{ILCH}.

Figure 8. External Clock Source Connections

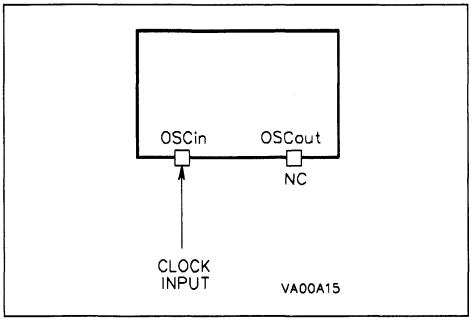


Figure 6. Equivalent Crystal Circuit

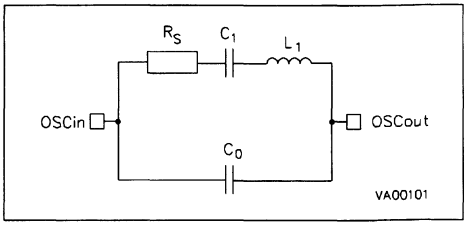
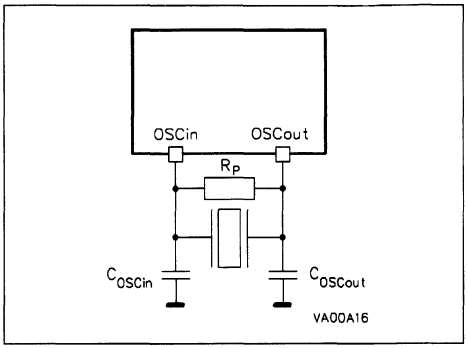


Figure 7. Crystal/Ceramic Resonator



Recommended Settings for Crystal

	2MHz	4MHz	8MHz	Unit
R_{SMAX}	400	75	60	Ω
C_0	5	7	10	pF
C_1	8	12	15	nF
C_{OSCin}	15-40	15-30	15-25	pF
C_{OSCout}	15-30	15-25	15-20	pF
R_P	10	10	10	MΩ
Q	30	40	60	

Recommended Settings for Ceramic Resonator

	2-8MHz	Unit
R_{SMAX}	10	Ω
C_0	40	pF
C_1	4.3	nF
C_{OSCin}	30	pF
C_{OSCout}	30	pF
R_P	1-10	MΩ
Q	1250	

1.8 RESETS AND INTERRUPTS

Resets are used to provide an orderly software startup procedure or to quit low power modes.

Two reset modes are provided: a power-on reset and an external reset at pin RESET.

A summary of the effects of both reset modes on the different sections of the MCU is given in Table 3. For further information, please refer to the part describing the particular section.

1.8.1 External Reset

The external reset is an active low input signal applied to the RESET pin of the MCU.

As shown in Figure 9, the RESET signal must stay low for a minimum of one and a half CPU clock cycles. A reset causes the reset vector to be fetched at addresses 3FFEh and 3FFFh in order to be loaded into the PC.

An internal Schmitt trigger at pin RESET improves noise immunity.

1.8.2 Power-on Reset (POR)

The power-on reset (POR) is generated upon detection of a positive transition on VDD (refer to Figure 9). It causes the reset vector to be fetched at addresses 3FFEh and 3FFFh in order to be loaded into the PC.

An internal circuitry provides a 4096 CPU clock cycle delay from the time the oscillator becomes active. At the end of the power-on reset, the MCU can be maintained in the reset condition by the external reset. The RESET pin can therefore be used to ensure V_{DD} has risen to a point where the MCU can properly operate before running the MCU program.

The power-on reset is strictly used for power up conditions and should not be used to detect any drop in the power supply voltage. There is no provision for a power-down reset.

Table 3. List of sections affected by RESET Power-on Reset (POR), WAIT and HALT

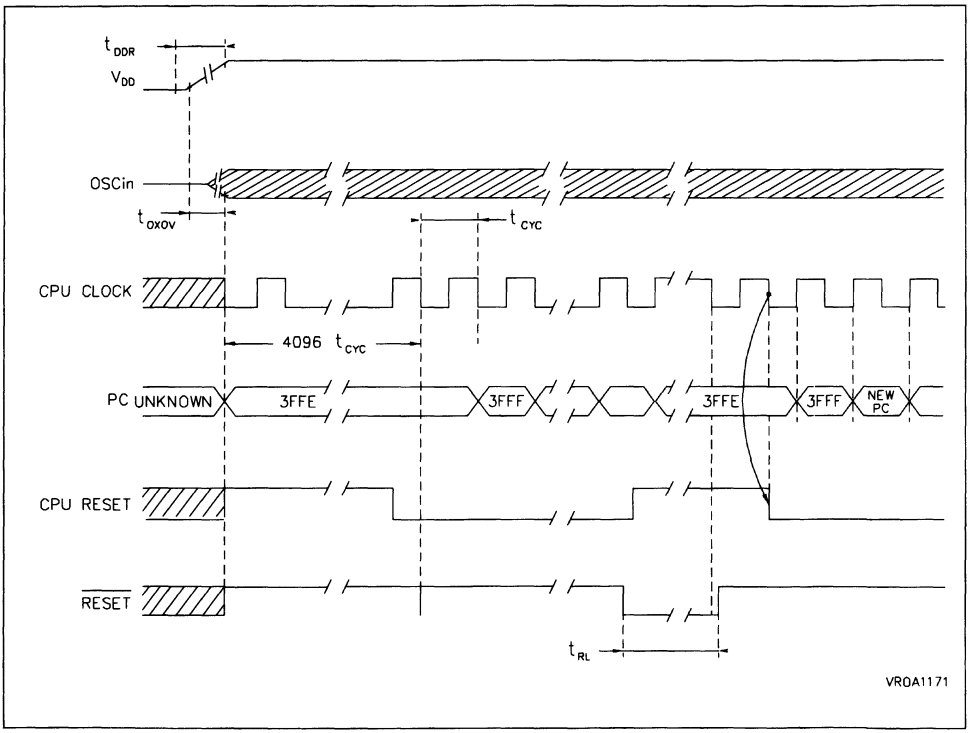
Section	RESET	POR	WAIT	HALT
Timer Prescaler reset to zero	X	X	-	-
Timer Counter set to FFFCh	X	X	-	-
All Timer enable bit set to 0 (disable)	X	X	-	-
Data Direction Registers set to 0 (as Inputs)	X	X	-	-
Set Stack Pointer to 00FFh	X	X	-	-
Force Internal Address Bus to restart vector 3FFEh, 3FFFh	X	X	-	-
Set Interrupt Mask Bit (I-Bit, CCR) to 1 (Interrupt Disable)	X	X	-	-
Set Interrupt Mask Bit (I-Bit, CCR) to 0 (Interrupt Enable)	-	-	X	X
Reset HALT Latch	X	X	-	-
Reset INT Latch	X	X	-	-
Reset WAIT Latch	X	X	-	-
Disable fop Clock (for 4096 cycles)	-	X	-	X
Set CPU Clock to 0	-	X	X	X
Set Timer Clock to 0	-	X	-	X

RESET AND INTERRUPTS (Continued)

1.8.3 Interrupts

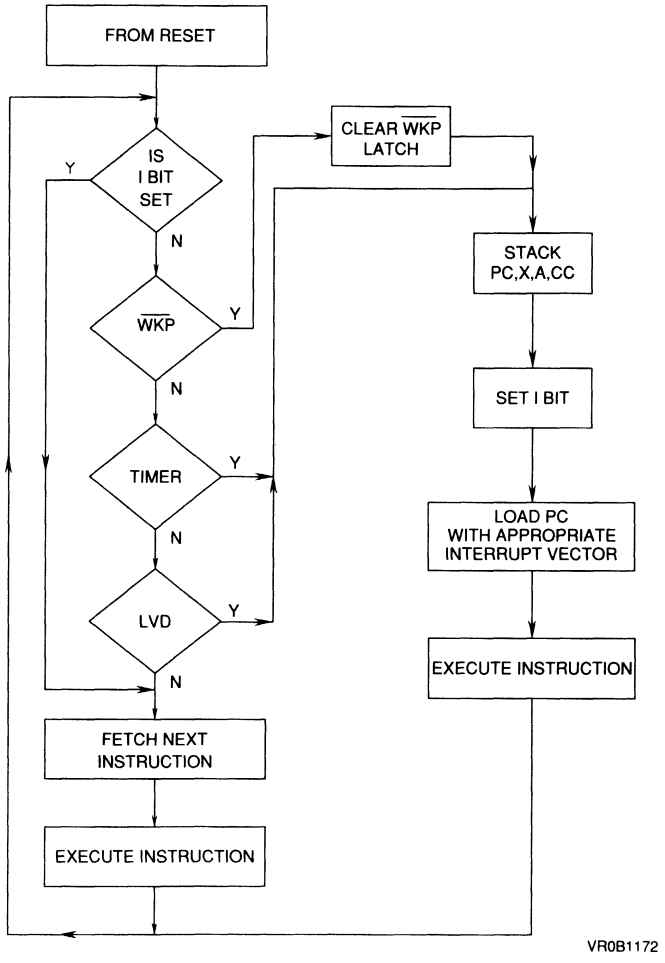
The ST7291 may be interrupted by one of five different methods: the three maskable hardware interrupts (WKP, TIMER and LVD) and the non-maskable software interrupt (TRAP). The Interrupt processing flowchart is shown in Figure 10. The maskable interrupts must be enabled in order to be serviced. However, disabled interrupts can be latched and processed when they are enabled. When an interrupt has to be serviced, the PC, X, A and CC registers are saved into the stack and the interrupt mask (I bit of the Condition Code Register) is set to prevent additional interrupts. The Y register is not automatically saved. The stack order is shown on Figure 3.

Figure 9. Reset Timing Diagram



RESET AND INTERRUPTS (Continued)

Figure 10. Interrupt Processing Flow-Chart



RESET AND INTERRUPTS (Continued)

The PC is then loaded with the interrupt vector of the interrupt to service and the interrupt service routine runs (refer to Table 4 for vector addresses). It should finish by the IRET instruction which causes the contents of the registers to be recovered from the stack and normal processing to resume. Note that the I bit is then cleared if and only if the corresponding bit stored in the stack is zero.

Though many interrupts can be simultaneously pending, a priority order is defined (see Table 2). The RESET pin has the highest priority. Then, if the I bit is low, the decreasing priority order is TRAP, WKP, timer and LVD. If the I bit is set, TRAP is the only enabled interrupt.

Interrupts allow the processor to leave low power modes. Refer to LOW POWER MODES for further information.

Software Interrupt. The software interrupt is the TRAP executable instruction. The interrupt is recognized when the TRAP instruction is executed, regardless to the I bit state. When the interrupt is recognized, it is serviced according to the flowchart on Figure 10.

External Interrupt. The external interrupt is generated through the WKP pin. The interrupt is enabled if the I bit of the CCR is cleared. An internal Schmidt trigger at pin WKP improves noise immunity.

The INT bit of the Miscellaneous Register (08h) allows selection of the interrupt triggering mode among the 2 available ones. Refer to Table 5 for the triggering mode coding.

When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution. It is then processed according to the flowchart on Figure 10.

If the interrupt is disabled (I high), the triggering edge of the WKP line is internally latched and the interrupt remains pending to be processed as soon as the interrupt is enabled (the low level sensitive interrupt is not latched and can therefore not remain pending). This internal latch is cleared in the first part of the service routine. Therefore, one, and one only, external interrupt can be latched and serviced as soon as enabled.

Figure 11 shows the mode timing diagram for the interrupt line. Two methods are described. The first method shows single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an IRET instruction occurs).

The second configuration shows several interrupt lines "wire-ORed" to form the interrupts at the processor. Thus, if after servicing one interrupt the interrupt line remains low, then the next interrupt is recognized.

Timer Interrupt. Two different timer interrupt flags are able to cause a timer interrupt when they are active if both the I bit of the CCR is reset and if the corresponding enable bit is set. If either of these conditions is false, the interrupt is latched and thus remains pending.

The interrupt flags are located in the Timer Status Register (0013h). The Enable bit are in the Timer Control Register (0012h).

When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution. it is then serviced according to the flowchart on Figure 10. Software in the timer service routine must determine the priority and cause of the timer interrupt by examining the interrupt flags and the status bits located in the TSR.

The general sequence for clearing an interrupt is an access to the status register while the flag is set followed by a read or write of an associated register. Note that the clearing sequence resets the internal latch. A pending interrupt (i.e. waiting for being enabled) will therefore be lost if the clear sequence is executed.

Refer to 16 BIT TIMER for further information.

RESET AND INTERRUPTS (Continued)

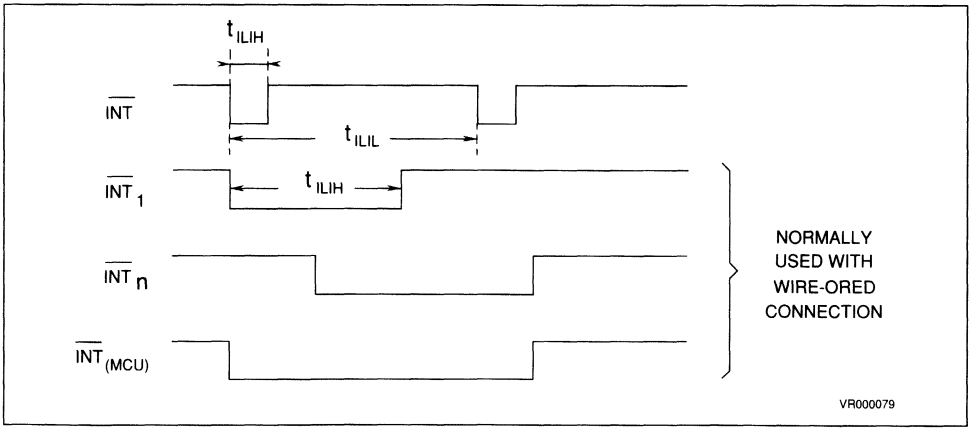
Table 4. Interrupt and Reset priorities

Vector Address	Interrupt Source	CPU Interrupt	Masked by	Priority
3FFEh,3FFFh	RESET and POWER-ON (POR)	RESET	none	Highest
3FFCh,3FFDh	SOFTWARE Interrupt (TRAP)	TRAP	none	↑
3FFAh,3FFBh	EXTERNAL Interrupt (WKP)	EXT. Int.	I-Bit	|
3FF8h,3FF9h	TIMER (OCF/TOF)	TIMER	I-Bit	|
3FF6h,3FF7h	MISCELLANEOUS	LVD	I-Bit	Lowest
3FF4h,3FF5h	Unused			
3FF2h,3FF3h	Unused			
3FF0h,3FF1h	Unused			

Table 5. External Interrupt

INT	External Interrupt
0	Falling edge only
1	Falling edge and low level

Figure 11. Timing Diagram for Interrupt Line



1.9 LOW POWER MODES

Table 1 gives a list of the different sections affected by the low power modes. For detailed information on a particular devices, please refer to the corresponding parts.

HALT Mode. The HALT mode is the MCU lowest power consumption mode. The HALT mode is entered by executing the HALT instruction. The internal oscillator is then turned off, causing all internal processing to be stopped, including the operation of the on-chip peripherals.

When entering the HALT mode, the I bit in the Condition Code Register is cleared. Thus, the external interrupts are allowed and the MCU is placed at its nominal speed (see CLOCK SYSTEM). All other registers and memory remain unaltered and all I/O lines remain unchanged.

The MCU can exit the HALT mode upon reception of either an external interrupt or PORTB or a power-on or external reset. The oscillator is then turned on and a stabilization time is provided before releasing CPU operation. The stabilization time is 4096 CPU clock cycles.

After the start up delay, the CPU continues operation by servicing the interrupt which wakes it up or by fetching the reset vector if a reset wakes it up.

Figure 12. HALT Function Flow Chart

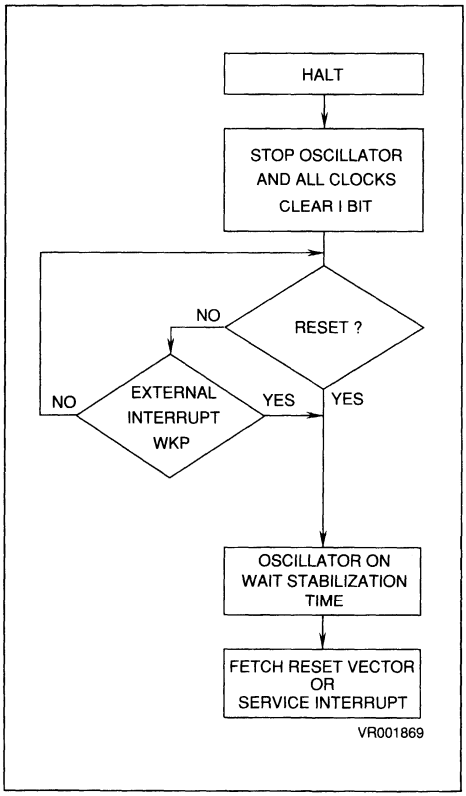
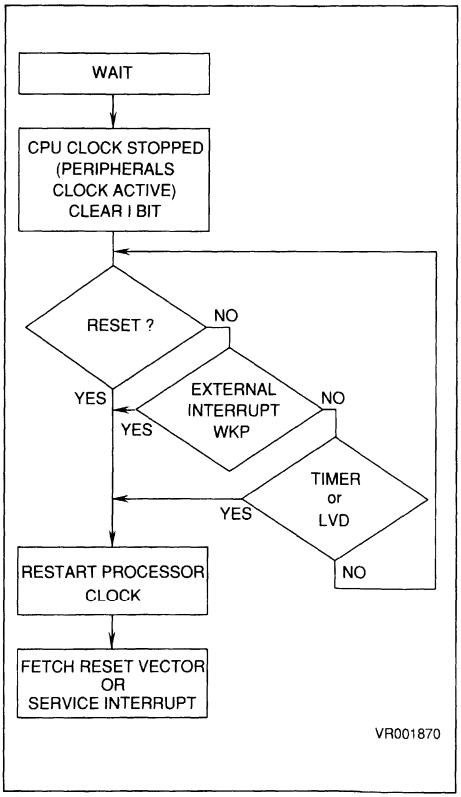


Figure 13. WAIT Flow Chart



LOW POWER MODES (Continued)

WAIT Mode. This mode is a low power consumption mode, but the power consumption is higher than in the HALT mode.

The WFI instruction places the MCU in the WAIT mode.

In the WAIT mode, the internal clock remains active but all CPU processing is stopped.

During the WAIT mode, the I bit in the condition code register is cleared to enable all interrupts. All other registers and memory remain unaltered and all parallel I/O lines remain unchanged.

An interrupt or a reset causes the MCU to exit the WAIT mode. An interrupt while the MCU is in the WAIT mode causes the corresponding interrupt vector to be fetched, the interrupt routine to be executed and normal processing to resume. A reset causes the program counter to fetch the reset vector and processing starts as for a normal reset.

DATA RETENTION Mode. The contents of RAM and CPU registers are retained at supply voltage as low as 2.0V. This is referred to as the data retention mode, where the data is held, but the device is not guaranteed to operate.

2 FUNCTIONS DESCRIPTION

2.1 I/O PORTS PROGRAMMING

2.1.1 Functional Description

Ports A, B are 8-bit I/O ports, port C is a 3-bit I/O port. Each of their pins can be individually configured under software control as either input or output.

Each bit of any DDR corresponds to an I/O pin of the associated port. A bit must be set to configure its associated pin as output and must be cleared to configure its associated pin as input. The Data Direction Registers can be written or read.

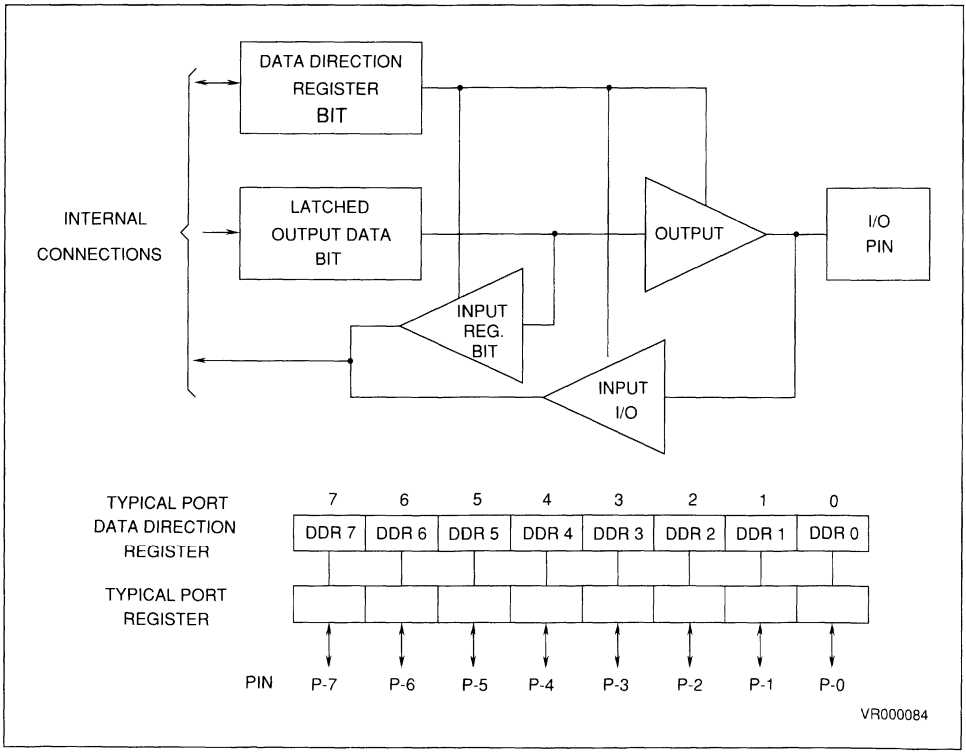
The typical I/O circuit is shown on Figure 14. Any write to an I/O port updates the port output register even if it is configured as input. Any read of an I/O port returns either the data latched in the port output register (output configured pins) or the value at the I/O pin (input configured pins) (see Table 6).

At power-on or external reset, all DDR's are cleared, which configures all port A, B and C pins as inputs, but the port output registers are not initialized. Thus, the I/O port should be written before setting the DDR bits to avoid undefined levels.

All unused I/O lines should be tied to an appropriate logic level (either V_{DD} or V_{SS}).

Port B: When WFD control bit is set, all I/O port B lines are tied to V_{DD} through WKP input.

Figure 14. I/O Pin Port A, Port C Typical Circuit



I/O PORTS PROGRAMMING (Continued)

Table 6. I/O Pin Functions

R/$\overline{W}$*	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

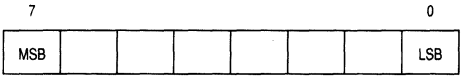
* R/$\overline{W}$ is an internal signal.

DATA REGISTERS

Port A: 00h
Port B: 01h
Port C: 02h

Read/Write

Reset Value: Undefined

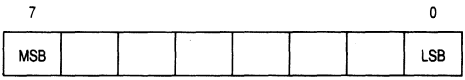


DATA DIRECTION REGISTERS

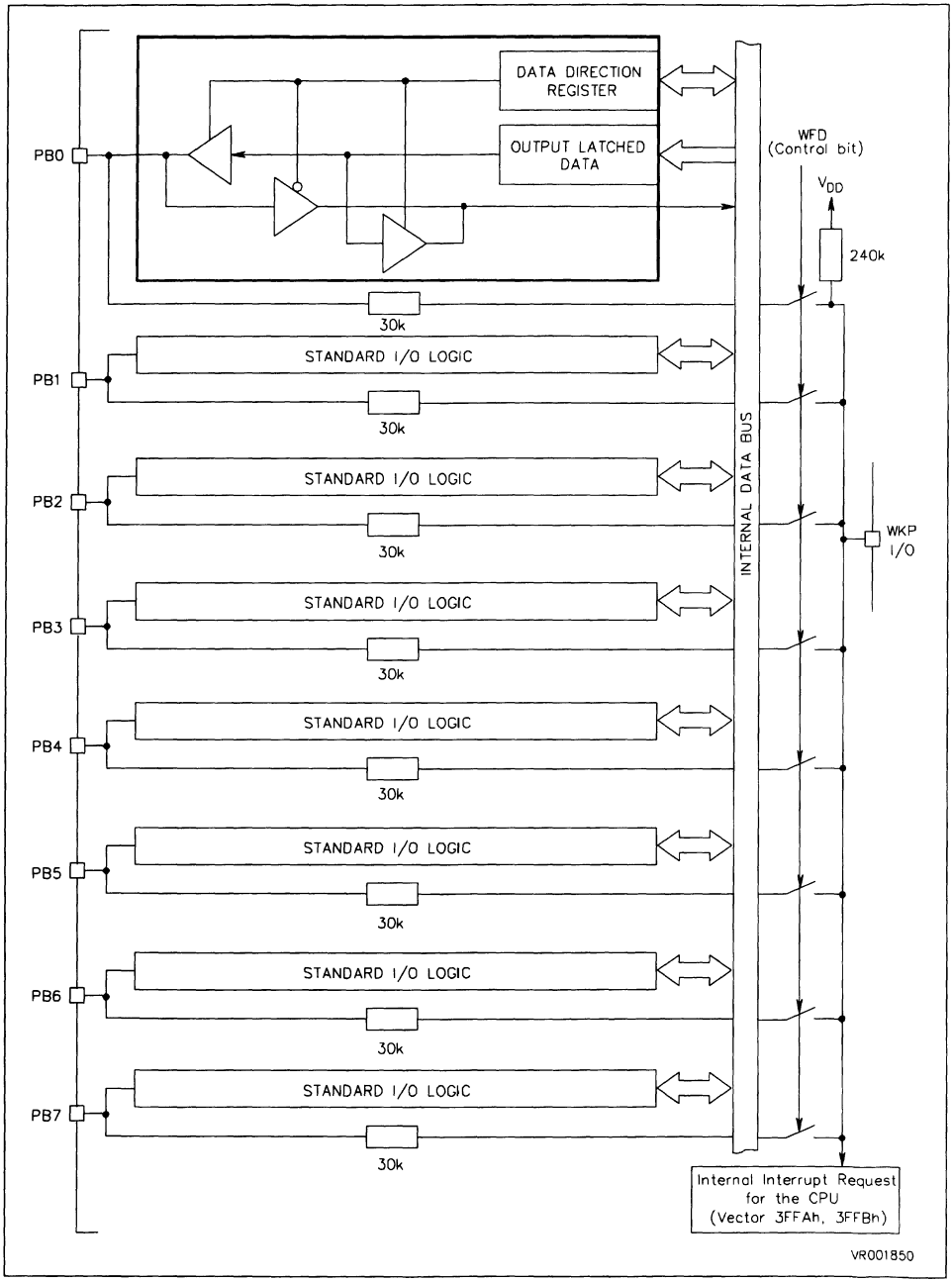
Port A: 04h
Port B: 05h
Port C: 06h

Read/Write

Reset Value: 00h (as inputs)



Example of Keyboard Interrupt



2.2 16 BIT TIMER

The 16-bit programmable timer consists of a 16-bit free running counter with one output compare register. It can be used for many purposes including pulse length measurement of one input signal and generation of one output waveform.

Pulse lengths and waveform periods can vary from several microseconds to many seconds because of the mask option configurable prescaler. When used with a 4MHz CPU clock, the timer has a resolution of 1µs.

Because the timer has a 16-bit architecture, each of its specific function block is represented by two registers. These registers contain the high order byte and low order byte of that function. However an access to the high order byte inhibits that specific timer capability until the low order byte is also accessed.

Note that correct software procedures should set the I bit of the Condition Code Register before accessing the high order byte to prevent an interrupt from occurring between the accesses to the high and low order bytes of any register.

The timer block diagram is shown on Figure 15:

2.2.1 Functional Description

Counter. The key element of the programmable timer is a 16-bit free running counter or counter register. It is preceded by a prescaler which divides the internal clock by four. This counter is incrementing by each event.

Software can read the counter at any time without affecting its value. It can be read from two locations, the Counter Register (0018h, 0019h) and Alternate Counter Register (001Ah, 001Bh). The only difference between these two read-only registers is the way the overflow flag TOF is handled during a read sequence.

A read sequence containing only a read of the least significant byte of the free running counter (from either the Counter Register or the Alternate Counter Register) will receive the LSB of the count value at the time of the read. A read of the most significant byte (from either the Counter Register or the Alternate Counter Register) simultaneously returns the MSB of the count value and causes the LSB to be transferred into a buffer.

The buffered value remains unchanged until the 16-bit read sequence is completed, even if the user reads the MSB several times. The read sequence is completed by reading the free running counter LSB, which actually returns the buffered value.

As shown on Figures 16 and 17, the free running counter is configured to FFFCh during reset. During a power-on reset (POR), the counter is also configured to FFFCh and begins running after the oscillator startup delay.

When the counter rolls over from FFFFh to 0000h, the Timer Overflow flag (TOF) of the Timer Status Register (TSR) is set. A timer interrupt is then generated if the TOIE enable bit of the Timer Control Register (TCR) is set, provided the I bit of the CCR is cleared. If one of these conditions is false, the interrupt remains pending to be issued as soon as they are both true. The interrupt request is cleared by reading TSR while TOF is set followed by an access (read or write) to the LSB of the Counter Register.

The TOF flag is not affected by accesses to the Alternate Counter Register. This feature allows simultaneous use of the overflow function and reads of the free running counter at random times (for example, to measure on elapsed time) without risking to clear the TOF flag erroneously. Accesses to the timer without the intention of servicing the TOF flag should therefore be performed to the Alternate Counter Register while only the TOF service routine accesses the Counter Register.

The value in the counter registers repeats every 262144 internal processor clock cycles. As shown on Figures 16, the counter increment is triggered by a falling edge of the CPU clock.

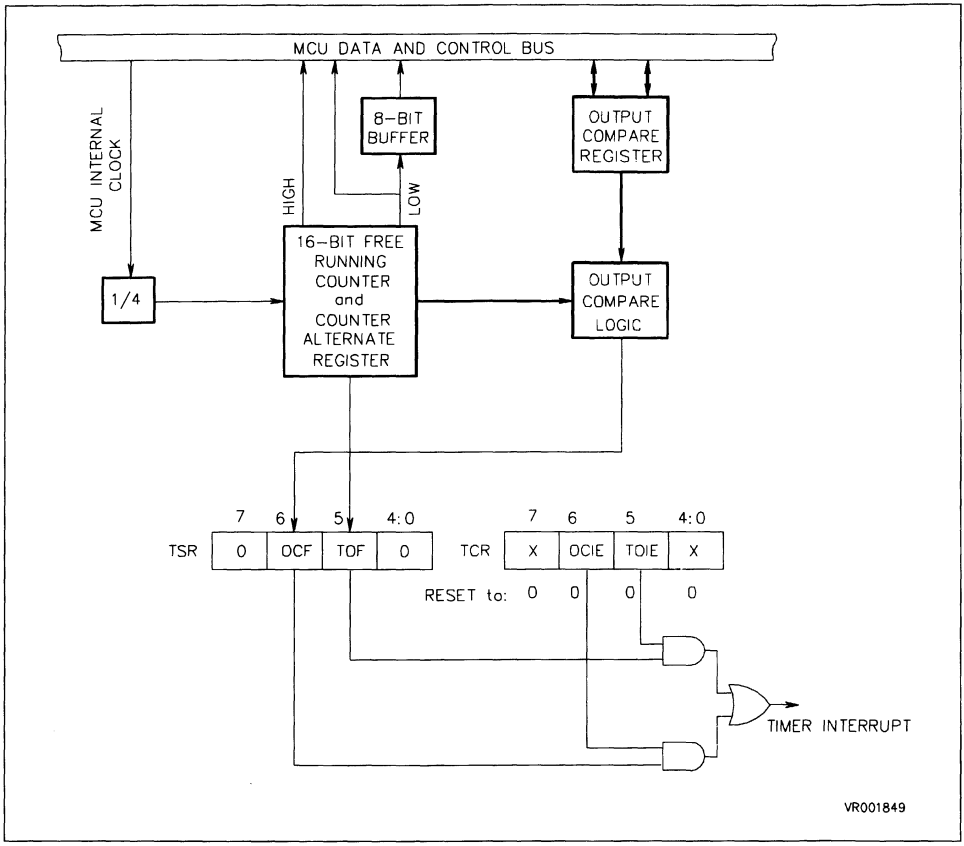
The timer is not affected by the WAIT mode. In the HALT mode, the counter stops counting until the mode is exited. Counting then resumes from previous count (MCU awaken by an interrupt) or from reset count (MCU awaken by a reset).

Output Compare. There is one output compare register but no output compare pin. It can be used for several purposes such as controlling an output waveform or indicating when a period of time has elapsed.

The Output Compare Register is unique because all bits are readable and writable and are not affected by the timer hardware and reset. If a compare function is not used, the two bytes of the Output Compare Register can be used as storage locations.

16 BIT TIMER (Continued)

Figure 15. Timer Block Diagram



The Output Compare Register (OCR) is a 16-bit register, which is made up of two 8-bit registers: The most significant byte register (OCHR) at address 0016h and the least significant byte register (OCLR) at address 0017h.

The content of OCR is compared with the content of the free running counter once during every timer clock cycles, i.e. once every 4 internal processor clock periods. If match is found, the Output Compare Flag OCF of the TSR is set.

An interrupt accompanies a successful output compare if the corresponding interrupt enable bit OCIE of the TCR is set, provided the I-bit of the CCR is cleared. Otherwise, the interrupt remains pending until both conditions are true. It is cleared by a read of TSR followed by an access to the LSB of the OCR.

After a processor write cycle to the OCHR register, the output compare function is inhibited until the OCLR is also written. Thus, the user must write both bytes if the MSB is written first. A write made to only the LSB will not inhibit the compare function.

The following procedure is recommanded to prevent the OCF flag from being set between the time it is read and the write to OCR.

Write to OCHR (further compares are inhibited).

Read the TSR (first step of the clearance of OCF [it may be already set]).

Write to OCLR (enables the output compare function and clears OCF).

16 BIT TIMER (Continued)

Figure 16. Timer Timing Diagram

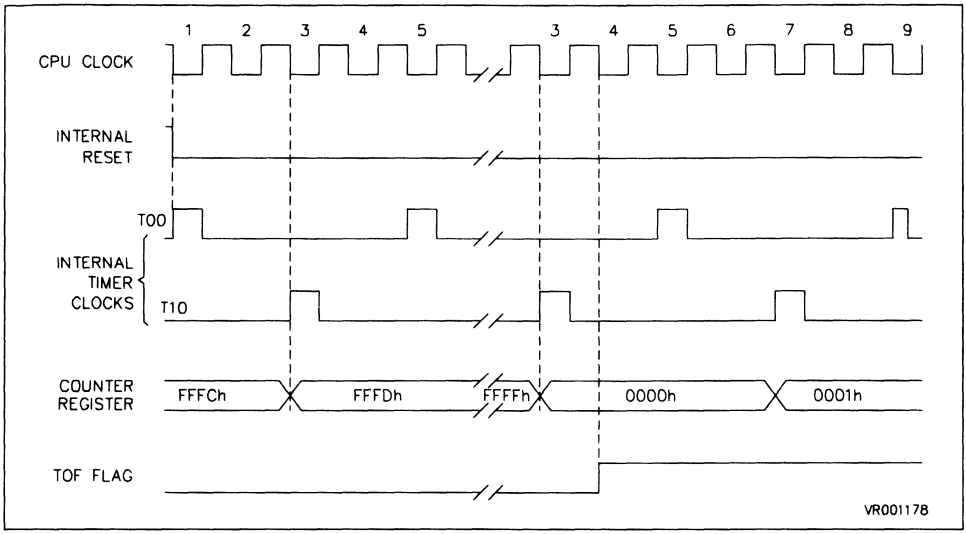
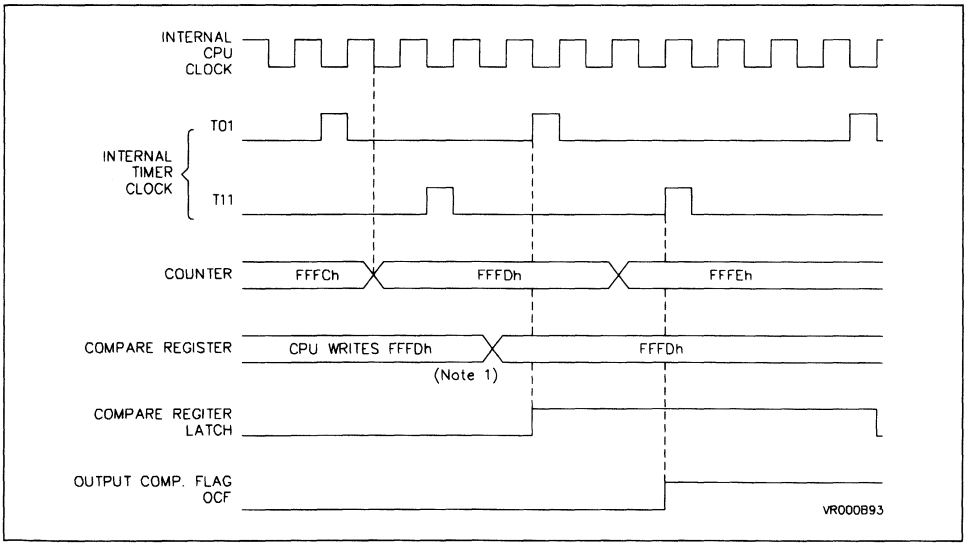


Figure 17. Output Compare Timing Diagram



Note 1: The CPU write to the compare registers may take place at any time but a compare only occurs at timer state T01. Thus a 4-cycle difference may exist between the write to the compare register and the actual compare.

16 BIT TIMER (Continued)

2.2.2 Timer Registers

TIMER CONTROL REGISTER (0012h)

Read/Write
Reset Value: 0000 0000 (00h)

The TCR is an 8 bit read/write register. Its eight bits are defined as follow:

7							0
0	OCIE	TOIE	0	0	0	0	0

Bit 6 = **OCIE** *Output Compare Interrupt Enable*
If OCIE is set, a timer interrupt is enabled whenever the OCF status flags of TSR are set. If the OCIE bit is cleared, the interrupt is inhibited.

Bit 5 = **TOIE** *Timer Overflow Interrupt Enable*
If TOIE is set, a timer interrupt is enable whenever the TOF status flag of TSR is set. If the TOIE bit is cleared, the interrupt is inhibited.

Bit 7, 4, 3, 2, 1, 0 = Unused, they are read to zero.

TIMER STATUS REGISTER (0013h)

Read Only
Reset Value: Undefined

The Timer Status Register (TSR) is an 8-bit register containing read-only status information.

7							0
0	OCF	TOF	0	0	0	0	0

Bit 6 = **OCF** *Output Compare Flag*
OCF is set when the content of the free running counter matches the content of OCR. It is cleared by a processor access of TSR while OCF is set followed by an access (read or write) to the low byte of OCR.

Bit 5 = **TOF** *Timer Overflow*
TOF is set by a transition of the free running counter from FFFFh to 0000h. It is cleared by a processor access to TSR while TOF is set followed by an access (read or write) to the low byte of the counter low register. TOF is not affected by an access to the Alternate Counter Register.

Bit 7, 4, 3, 2, 1, 0 = Unused

3 SOFTWARE AND CHARACTERISTICS

3.1 SOFTWARE DESCRIPTION

3.1.1 Instruction Set

The ST7 instruction set is an 8 bit industry standard instruction set that can be divided into five major groups. All instructions of each group have the same addressing modes. Refer to ST7 MACRO ASSEMBLER USER'S GUIDE and ST7 PROGRAMMING MANUAL for detailed information.

Group 1 : Register/Memory And Absolute Jump Group In this group most instructions contain two operands. One operand is inherently defined as either the accumulator or an index register. The other operand is fetched from memory using one of the allowed addressing modes. The absolute jump instructions are included in this group because they can use most of the addressing modes of the register/memory instructions.

Examples: LD <ea>, a. This means that the memory byte located at address <ea> is loaded with the 8-bit content of the accumulator A.

The list of the instructions of this group is given in Table 7.

Group 2 : Read - Modify - Write Group These instructions read a register or a memory location, modify its content and write the new value back.

Example : RRC <ea>. This means that the content of the memory byte located at address <ea> is rotated right through the carry bit, the result is written in the memory <ea> and the carry bit.

The list of the instructions of this group is given in Table 8.

Group 3 : Bit Manipulation And Test Group Bit manipulation instructions can set or clear any bit within the first 256 memory locations, except for ROM (020h - 04F) and read-only registers located at addresses 03h, 07h, 09h to 11h, 14h, 15h, 1Ch to 1Fh.

Example: BSET <ea>, #b. This sets the bit #b of memory location <ea>.

Test instructions can test any bit of the first 256 memory locations and jump conditional within an 8 bit PC-relative displacement.

Example: BTJT <ea>, #b, ee. This corresponds to the relative jump (displacement = ee) if bit number #b of memory location <ea> is set. (Bit test and jump if true).

The list of the instructions of this group is given in Table 9.

Group 4 : PC-Relative Jump Group These instructions execute a PC-relative jump (8-bit displacement) depending on the state of the flag bits inside the condition code register (H, I, N, Z, C flags).

Example: JRC ee. This means jump with displacement ee from actual the PC value if the carry bit is set, else execute the next instruction.

The list of the instructions of this group is given in Table 10.

Group 5 : Miscellaneous Group These instructions are mainly control instructions on registers, stack, interrupts, subroutines and power down modes.

The multiply instruction is included in this group. It performs an 8 x 8 bit unsigned multiplication between one index register and the accumulator. The result is given as 16 bits, with the high order byte in the index register and the low order one in the accumulator.

The list of the instructions of this group is given in Table 11.

3.1.2 Addressing Modes

The CPU uses 10 main addressing modes to provide the programmer with an opportunity to optimize his code in most applications.

The various indexed addressing modes make it possible to locate data labels, code conversion tables and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions, while the longest instructions (three bytes) allow access of tables throughout memory.

Short absolute (direct) and long absolute (extended) addressing modes are also included. Extended addressing permits jump instructions to reach all memory.

The various addressing modes differ from each other in computing the effective address (EA) i.e. in calculating the address to or from which the argument of an instruction is fetched or stored. The LSBEA is the least significant byte of the EA; the MSBEA is its most significant byte. The 16 addressing modes of the processor are described below.

The table of symbols is given in Table 8 while the effective address coding is given in Table 7.

SOFTWARE DESCRIPTION (Continued)

In order to extend the number of op-codes available for an eight bit CPU (256 op-codes), three "pre-byte" op-codes have been defined. These pre-byte have to be seen as pre-instructions that modify the meaning of the instruction they precede. The whole instruction becomes:

PC-1 End of previous instruction

PC Pre-byte

PC + 1 Op-code

PC + 2 Additional word (0 to 2) according to the number of byte required to compute the effective address.

The pre-bytes enable instructions in Y as well as indirect addressing modes to be implemented. They precede the opcode of the instruction in X or of the instruction using a direct addressing mode. The pre-bytes are :

PDY : 90h Transform an instruction in X using immediate, direct, indexed, direct bit or inherent addressing modes to an instruction in Y using the same addressing mode.

PIY : 91h Transform an instruction using X indexed addressing mode to an instruction using indirect Y indexed addressing mode.

PIX : 92h Transform an instruction using direct, direct bit or direct relative addressing mode to an instruction using the corresponding indirect addressing mode. It also transforms an instruction using X indexed addressing mode to an instruction using indirect X indexed addressing mode.

The pre-byte is completely user transparent. It is part of the assembly code.

The addressing modes are discussed in the following paragraphs.

Table 7. Source Coding

Addressing Mode	Source Coding	Example
Immediate	#nn	LD a, #0Ah
Direct	ad8	LD a, 0Ah
Extended	ad16	LD a, 10EAh
Indexed no offset	(iX)	LD a, (X)
Indexed 8 bit offset	(d8, iX)	LD a, (1Bh, Y)
Indexed 16 bit offset	(d16, iX)	LD a, (100Ah, X)
Memory indirect short	[ad8]	LD a, [1Bh]
Memory indirect long	[ad16]	LD a, [100Ah]
Memory indirect short indexed	([ad8], iX)	LD a, ([1Bh], X)
Memory indirect long indexed	([ad16], iX)	LD a, ([100Ah], Y)

Table 8. Table of Symbols

a	Accumulator	nn	8 bit immediate value
iX	Index register (either Xo r Y)	ad8	8 bit address
X	X index register	ad16	16 bit address
Y	Y index register	d8	8 bit signed offset
S	Stack pointer	d16	16 bit signed offset
CC	Condition code register	ee	8 bit PC relative displacement
<ea>	Effecive address	b	3 bit number

SOFTWARE DESCRIPTION (Continued)

Inherent. In inherent instructions, there is no EA as there is no operand to fetch or store. All the information needed to execute the instruction is contained in the op-code. Operations specifying only an index register or the accumulator, and no other arguments, are included in this mode.

Immediate. In immediate addressing the operand is stored in the byte immediately following the op-code.

Direct Modes

Direct. In the direct addressing mode, the effective address is contained in a single byte following the op-code byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction.

Extended. In the extended addressing mode, the effective address of the argument is contained in the two bytes following the op-code. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory.

Indexed Modes

Indexed Without Offset. In the indexed without offset addressing mode, the effective address is contained in one index register (X or Y). This addressing mode can therefore access the first 256 memory locations. These instructions are only one byte long.

This mode is mainly used to move a pointer through a table or to address a frequently referenced RAM or I/0 location.

Indexed 8 Bit Offset. The EA is obtained by adding the 8-bit unsigned contents of the second instruction byte to the 8-bit unsigned content of the appropriate index register. This mode allows addressing of 256 locations of the 511 lowest memory locations.

Indexed 16 Bit Offset. The EA is obtained by adding the 16-bit unsigned value composed of the second (MSB) and the third (LSB) instruction bytes to the 8-bit unsigned content of the appropriate **index register**. This mode allows addressing of 256 locations anywhere in the memory map.

Indirect Modes

Short Indirect. In this mode, the second byte of the instruction is used as a page zero address. The content of this page zero memory location is the LSB of the effective address. The MSBEA is zero (i.e. the effective address points to a page zero location).

Long Indirect. In the long indirect mode, the second byte of the instruction is used as a page zero pointer. The MSBEA is the content of this location while the LSBEA is the content of the following page zero location.

Indirect Indexed Modes

Short Indirect Indexed. The second byte of the instruction is used as a page zero address. To obtain the LSBEA, the content of this page zero memory location is added to the 8- bit unsigned value contained in the specified index register. The MSBEA is zero (i.e. the effective address points to a page zero location).

Long Indirect Indexed. In long indirect indexed mode, the second byte of the instruction is used as a page zero pointer. The 16-bit word read from this location (MSB at the pointed address and LSB at the following one) is added to the 8-bit unsigned value contained in the specified index register to form the 16-bit EA.

Relative Modes

Simple Relative. The relative addressing mode is used for branch instruction (e.g. Branch on bit, Branch on condition, Branch subroutine). The branch address (new value of PC) is calculated by adding a displacement given by the 8-bit signed byte following the op-code value to the actual content of the PC. This means that the variation of PC value is in the range -126 to +127 from the op-code address (the offset value can be calculated by the assembler).

Indirect Relative. The indirect relative addressing mode is similar to the relative mode but the content of the second byte of the instruction is used as a page zero address containing the 8-bit signed displacement value to be added to the actual content of the PC (i.e. address of the op-code plus 2).

SOFTWARE DESCRIPTION (Continued)

Direct Bit Modes

Bit Set And Clear. Bit Set/Clear mode is used to read-modify-write one single bit of a memory location in page zero, including I/O bits. The concerned memory location is given by the byte following the op-code (direct addressing mode) while the position of the bit to deal with is given in 3 bits included in the op-code.

Bit Test And Branch. Bit test and branch mode gives a relative branch according to the value of a single bit of a memory location in page zero. The op-code contains 3 bits to define the bit to test at a location given by the byte immediately following the op-code. A third byte gives the 8-bit signed value of the PC-relative displacement. If the test is true, this displacement is added to the actual content of the PC (i.e. op-code address plus 2) to form the new value of the PC.

Indirect Bit Modes

Indirect Bit Set And Clear. Indirect Bit Set/Clear mode works similarly to the bit Set/Clear mode except that the address of the concerned byte is the content of the location pointed by the second byte of the instruction.

Indirect Bit Test And Branch. This mode works as the bit test and branch mode but the tested byte is the content of the location pointed by the second byte of the instruction.

SOFTWARE DESCRIPTION (Continued)

Example

FUNCTION	SOURCE CODING	ADDRESSING MODES
		Immediate
Load a with memory	LD a,<ea>	2 A6 [2]

# Bytes	OP-Code	# Cycles

Table 9. Register/Memory and Absolute Jump Group

FUNCTION	SOURCE CODE	ADDRESSING MODE					
		Immediate	Direct	Extended	Index 0	Index 8	Index 16
Load A with memory	LD a,<ea>	2 A6 [2]	2 B6 [3]	3 C6 [4]	1 F6 [3]	2 E6 [4]	3 D6 [5]
Load iX with memory	LD iX,<ea>	2 AE [2]	2 BE [3]	3 CE [4]	1 FE [3]	2 EE [4]	3 DE [5]
Load memory with A	LD <ea>,a	—	2 B7 [4]	3 C7 [5]	1 F7 [4]	2 E7 [5]	3 D7 [6]
Load memory with iX	LD <ea>,iX	—	2 BF [4]	3 CF [5]	1 FF [4]	2 EF [5]	3 DF [6]
Add memory to A	ADD a,<ea>	2 AB [2]	2 BB [3]	3 CB [4]	1 FB [3]	2 EB [4]	3 DB [5]
Add memory and carry to A	ADC a,<ea>	2 A9 [2]	2 B9 [3]	3 C9 [4]	1 F9 [3]	2 E9 [4]	3 D9 [5]
Subtract memory to A	SUB a,<ea>	2 A0 [2]	2 B0 [3]	3 C0 [4]	1 F0 [3]	2 E0 [4]	3 D0 [5]
Subtract memory with carry	SBC a,<ea>	2 A2 [2]	2 B2 [3]	3 C2 [4]	1 F2 [3]	2 E2 [4]	3 D2 [5]
And memory to A	AND a,<ea>	2 A4 [2]	2 B4 [3]	3 C4 [4]	1 F4 [3]	2 E4 [4]	3 D4 [5]
Or memory with A	OR a,<ea>	2 AA [2]	2 BA [3]	3 CA [4]	1 FA [3]	2 EA [4]	3 DA [5]
Exclusive OR	XOR a,<ea>	2 A8 [2]	2 B8 [3]	3 C8 [4]	1 F8 [3]	2 E8 [4]	3 D8 [5]
Arithmetic Compare A	CP a,<ea>	2 A1 [2]	2 B1 [3]	3 C1 [4]	1 F1 [3]	2 E1 [4]	3 D1 [5]
Arithmetic Compare iX	CP iX,<ea>	2 A3 [2]	2 B3 [3]	3 C3 [4]	1 F3 [3]	2 E3 [4]	3 D3 [5]
Bit compare A and memory	BCP a,<ea>	2 A5 [2]	2 B5 [3]	3 C5 [4]	1 F5 [3]	2 E5 [4]	3 D5 [5]
Absolute Jump	JP <ea>	—	2 BC [2]	3 CC [3]	1 FC [2]	2 EC [3]	3 DC [4]
Call subroutine	CALL <ea>	—	2 BD [5]	3 CD [6]	1 FD [5]	2 ED [6]	3 DD [7]

SOFTWARE DESCRIPTION (Continued)

Table 10. Read - Write Group

FUNCTION	SOURCE CODE	ADDRESSING MODE						
		Inh a	Inh iX	Direct	Memory Direct	Index 0	Index +d8	Index +[ad8]
Increment	INC <ea>	1 4C [3]	1 5C [3]	2 3C [5]	3 923C [7]	1 7C [5]	2 6C [6]	3 926C [8]
(Y index)			2 905C [4]		3 913C [7]	2 907C [6]	3 906C [7]	3 916C [8]
Decrement	DEC <ea>	1 4A [3]	1 5A [3]	2 3A [5]	3 923A [7]	1 7A [5]	2 6A [6]	3 926A [8]
(Y index)			2 905A [4]			2 907A [6]	3 906A [7]	3 916A [8]
Clear	CLR <ea>	1 4F [3]	1 5F [3]	2 3F [5]	3 923F [7]	1 7F [5]	2 6F [6]	3 926F [8]
(Y index)			2 905F [4]			2 907F [6]	3 906F [7]	3 916F [8]
One's Complement	CPL <ea>	1 43 [3]	1 53 [3]	2 33 [5]	3 9233 [7]	1 73 [5]	2 63 [6]	3 9263 [8]
(Y index)			2 9053 [4]			2 9073 [6]	3 9063 [7]	3 9163 [8]
Negate (2's complement)	NEG <ea>	1 40 [3]	1 50 [3]	2 30 [5]	3 9230 [7]	1 70 [5]	2 60 [6]	3 9260 [8]
(Y index)			2 9050 [4]			2 9070 [6]	3 9060 [7]	3 9160 [8]
Rotate Left thru Carry	RLC <ea>	1 49 [3]	1 59 [3]	2 39 [5]	3 9239 [7]	1 79 [5]	2 69 [6]	3 9269 [8]
(Y index)			2 9059 [4]			2 9079 [6]	3 9069 [7]	3 9169 [8]
Rotate Right thru Carry	RRC <ea>	1 46 [3]	1 56 [3]	2 36 [5]	3 9236 [7]	1 76 [5]	2 66 [6]	3 9266 [8]
(Y index)			2 9056 [4]			2 9076 [6]	3 9066 [7]	3 9166 [8]
Shift Left Logical	SLL <ea>	1 48 [3]	1 58 [3]	2 38 [5]	3 9238 [7]	1 78 [5]	2 68 [6]	3 9268 [8]
(Y index)			2 9058 [4]			2 9078 [6]	3 9068 [7]	3 9168 [8]
Shift Right Logical	SRL <ea>	1 44 [3]	1 54 [3]	2 34 [5]	3 9234 [7]	1 74 [5]	2 64 [6]	3 9264 [8]
(Y index)			2 9054 [4]			2 9074 [6]	3 9064 [7]	3 9164 [8]
Shift Left Arithmetic	SLA <ea>	1 48 [3]	1 58 [3]	2 38 [5]	3 9238 [7]	1 78 [5]	2 68 [6]	3 9268 [8]
(Y index)			2 9058 [4]			2 9078 [6]	3 9068 [7]	3 9168 [8]
Shift Right Arithmetic	SRA <ea>	1 47 [3]	1 57 [3]	2 37 [5]	3 9237 [7]	1 77 [5]	2 67 [6]	3 9267 [8]
(Y index)			2 9057 [4]			2 9077 [6]	3 9067 [7]	3 9167 [8]
Test for Negative or Zero	TNZ <ea>	1 4D [3]	1 5D [3]	2 3D [4]	3 923D [6]	1 7D [4]	2 6D [5]	3 926D [7]
(Y index)			2 905D [4]			2 907D [5]	3 906D [6]	3 916D [7]
Swap Nibbles	SWAP <ea>	1 4E [3]	1 5E [3]	2 3E [5]	3 923E [7]	1 7E [5]	2 6E [6]	3 926E [8]
(Y index)			2 905E [4]			2 907E [6]	3 906E [7]	3 916E [8]

SOFTWARE DESCRIPTION (Continued)

Table 11. Bit Manipulation And Test Group

FUNCTION	SOURCE CODE	ADDRESSING MODES	
		Relative	Indirect Relative
Bit Set	BSET <ea> , # b	2 (10+2*b) [5]	3 92(10+2*b) [7]
Bit Reset	BRES <ea> , # b	2 (11+2*b) [5]	3 92(10+2*b) [7]
Bit Test and Jump if True	BTJT <ea> , # b , ee	3 (00+2*b) [5]	4 92(00+2*b) [7]
Bit Test and Jump if False	BTJF <ea> , # b , ee	3 (01+2*b) [5]	4 92(01+2*b) [7]

Table 12. PC-Relative Jump Group

FUNCTION	SOURCE CODE	ADDRESSING MODES	
		Relative	Indirect Relative
Jump Relative True	JRT ee	2 20 [3]	3 9220 [5]
(Jump Relative always)	JRA ee	2 20 [3]	3 9220 [5]
Jump Relative False	JRF ee	2 21 [3]	3 9221 [5]
Jump Relative if Unsigned Greater than	JRUGT ee	2 22 [3]	3 9222 [5]
Jump Relative if Unsigned Lower or Equal	JRULE ee	2 23 [3]	3 9223 [5]
Jump Relative if No Carry	JRNC ee	2 24 [3]	3 9224 [5]
Jump Relative if Unsigned Greater or Equal	JRUGE ee	2 24 [3]	3 9224 [5]
Jump Relative if Carry	JRC ee	2 25 [3]	3 9225 [5]
Jump Relative if Unsigned Lower than	JRULT ee	2 25 [3]	3 9225 [5]
Jump Relative if Not Equal	JRNE ee	2 26 [3]	3 9226 [5]
Jump Relative if Equal	JREQ ee	2 27 [3]	3 9227 [5]
Jump Relative if Half Carry	JRH ee	2 28 [3]	3 9228 [5]
Jump Relative if Not Half Carry	JRNH ee	2 29 [3]	3 9229 [5]
Jump Relative if Plus	JRPL ee	2 2A [3]	3 922A [5]
Jump Relative if Minus	JRMI ee	2 2B [3]	3 922B [5]
Jump Relative if Not Interrupt Mask	JRNM ee	2 2C [3]	3 922C [5]
Jump Relative if Interrupt Mask	JRM ee	2 2D [3]	3 922D [5]
Jump Relative if Interrupt Line Low	JRIL ee	2 2E [3]	3 922E [5]
Jump Relative if Interrupt Line High	JRIH ee	2 2F [3]	3 922F [5]
Call Subroutine Relative	CALLR ee	2 AD [6]	3 92AD [8]

SOFTWARE DESCRIPTION (Continued)

Table 13. Miscellaneous Group

FUNCTION	SOURCE CODE	X iNDEX
Multiply (iX, A = iX * A)	MUL iX , a	+ 42 [11]
Load iX with acc. a content	LL iX , a	+ 97 [2]
Load a with iX content	LL a , iX	+ 9F [2]
Load Stack p. with acc. a content	LD S , a	+ 95 [2]
Load acc. a with Stack p. content	LD a , S	+ 9E [2]
Load Stack p. with iX content	LD S , iX	+ 94 [2]
Load iX with Stack p. content	LD iX , S	+ 96 [2]
Load X // with Y // content	LD X , Y	+ 93 [2]
Load Y // with X // content	LD Y , X	—
Push acc. a onto the Stack	PUSH A	+ 88 [3]
Pop acc. a from the Stack	POP A	+ 84 [4]
Push iX onto the stack	PUSH iX	+ 89 [3]
Pop iX from the Stack	POP iX	+ 85 [4]
Push Condition Codes onto the Stack	PUSH CC	+ 8A [3]
Pop Condition Codes from the Stack	POP CC	+ 86 [4]
Reset Carry Flag	RCF	+ 98 [2]
Set Carry Flag	SCF	+ 99 [2]
Reset Interrupt Mask	RIM	+ 9A [2]
Set Interrupt Mask	SIM	+ 9B [2]
Reset Stack Pointer	RSP	+ 9C [2]
No Operation	NOP	+ 9D [2]
Interrupt Routine Return	IRET	+ 80 [9]
Subroutine Return	RET	+ 81 [6]
Software Trap	TRAP	+ 83 [10]
Halt	HALT	+ 8E [2]
Wait For Interrupt	WFI	+ 8F [2]

3.2 ELECTRICAL CHARACTERISTICS

Power Considerations

T_J, the average chip-junction temperature in Celsius can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta JA) \quad (1)$$

Where:

- T_A is the Ambient Temperature in °C,
- θJA is the Package Thermal Resistance, Junction-to-Ambient in °C/W,
- P_D the sum of P_{INT} and $P_{I/O}$,
- P_{INT} equals I_{CC} time V_{CC}, Watts-Chip Internal Power
- $P_{I/O}$ the Power Dissipation on Input and Output Pins, User Determined.

For most applications $P_{I/O} < P_{INT}$ and can be neglected .

P_{PORT} may be significant if the device is configured to drive Darlington bases or sink LED Loads.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K + (T_J + 273°C) \quad (2)$$

Therefore :

$$K = P_D \times (T_A + 273°C) + \theta JA \times P_D^2 \quad (3)$$

Where K is constant pertaining to the particular part, K can be determined from equation (3) by measuring P_D (at equilibrium) for a kwon T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

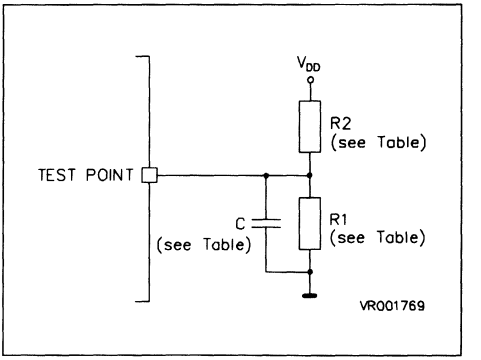
Thermal Characteristics

Symbol	Characteristics	Value	Unit
θJA	Thermal Resistance PDIP28 PSO28	 47 50	°C/W

Equivalent Test Load

V_{DD} = 3V			
Pins	**R1**	**R2**	**C**
PA0-PA7 PB0-PB7 PC1, PC6, PC7	10.91kΩ	6.32kΩ	50pF
V_{DD} = 4.5V			
Pins	**R1**	**R2**	**C**
PA0-PA7 PB0-PB7 PC1, PC6, PC7	3.26kΩ	2.38kΩ	50pF

Test Diagram



AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD}	Operating Supply Voltage	RUN Mode HALT Mode WAIT Mode	3.0 3.0 3.0		5.5	V
I_{DD}	Supply Current [1] [2] [3]	RUN Mode V_{DD}=5V,f_{OSC}=4MHz V_{DD}=5V,f_{OSC}=8MHz V_{DD}=3.3V,f_{OSC}=4MHz WAIT Mode V_{DD}=5V,f_{OSC}=4MHz V_{DD}=5V,f_{OSC}=8MHz V_{DD}=3.3V,f_{OSC}=4MHz HALT Mode V_{DD}=5V,T_A=70°C			 5 10 3 3 6 1.8 10	 mA mA mA mA mA mA µA

Notes:

1. RUN (Operating) IDD, WAIT I_{DD} measured using external square wave clock all inputs 0.2V from rail, no DC load, less than 50pF on all outputs, CI = 20pF on OSCout.
2. WAIT, HALT all I/O configured as inputs, V_{IL} = 0.2V, V_{IH} = V_{DD}-0.2V.
3. HALT, OSCin = V_{SS}.

DC Electrical Characteristics

Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Output Voltage, Load ≤ 10.0µA			0.1	V
V_{OH}		V_{DD}-0.1			V
	Output High Voltage				
V_{OH}	I LOAD =1.6mA, PA0-PA7,PB0-PB7,PC1,PC6,PC7 at V_{CC}=5V	V_{DD}-0.8			V
	I LOAD =0.4mA, PA0-PA7,PB0-PB7,PC1,PC6,PC7 at V_{CC}=3.3V	V_{DD}-0.3			V
V_{OL}	Output Low Voltage				V
	I LOAD =1.6 mA, PA0-PA7,PB0-PB5,PC1-PC6,PC7 at V_{CC}=5V			0.3	V
	I LOAD =0.4 mA, PA0-PA7,PB0-PB5,PC1-PC6,PC7 at V_{CC}=3.3V			0.3	V
V_{IH}	Input High Voltage				
	PA0-PA7,PB0-PB7,PC1,PC6,PC7,$\overline{WKP}$,$\overline{RESET}$	0.7xV_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage				
	PA0-PA7,PB0-PB7,PC1,PC6,PC7,$\overline{WKP}$,$\overline{RESET}$	V_{SS}		0.2xV_{DD}	V
V_{RM}	Data Retention Mode (0 to 70°C)	2			V
I_{IL}	I/O Ports Hi-Z Leakage Current				
	PA0-PA7,PB0-PB7,PC1,PC6,PC7			± 10	µA
I_{IN}	Input Current : $\overline{RESET}$, $\overline{WKP}$, OSCin			± 1	µA
C_{OUT}	Capacitance : Ports (as Input or Output)			12	pF
C_{IN}	$\overline{RESET}$, $\overline{WKP}$			8	pF
V_{LVD}	Low Voltage Detector Threshold	3.1	3.5	3.8	V
R_{PB} (1)	Port B Wake-up Resistor	20	30	40	kΩ
R_{WKP} (1)	$\overline{WKP}$ Pull-up	160	240	320	kΩ

Note 1. The ration between RWKP and RPB is 8 ± 10%

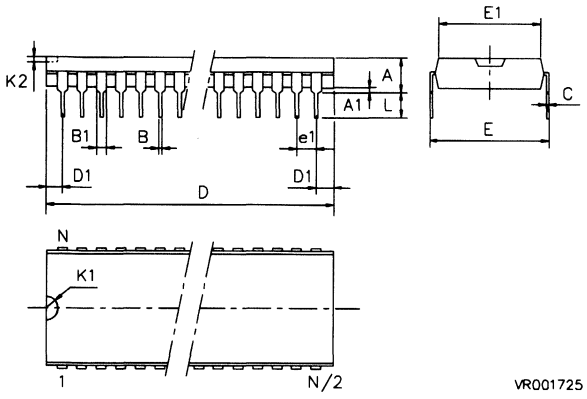
CONTROL TIMING

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Frequency of Operation	V_{DD}=5V V_{DD}=3.3V	DC DC		8 4	MHz
t_{ILCH}	HALT Mode Recovery Startup Time	Crystal Oscillator			50	ms
t_{RL}	External RESET Input Pulse Width		1.5			t_{CYC}
t_{ILIH}	Interrupt Pulse Width WKP PORTB		 125 125			ns
t_{ILIL}	Interrupt Pulse Period		(1)			t_{CYC}
t_{OXOV}	Crystal Oscillator Startup Time				50	ms
t_{DDR}	Supply Rise Time	10% to 90%	0.01		100	ms

Note 1. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 cycles.

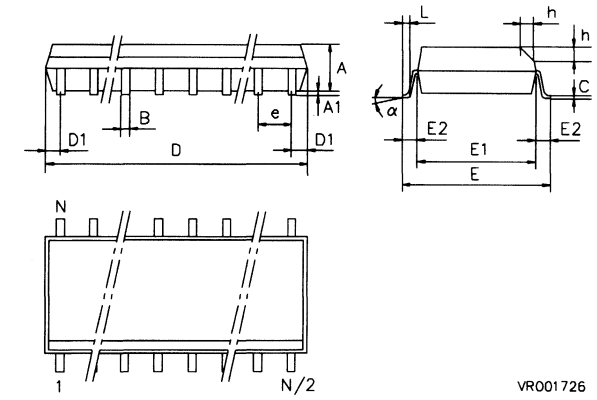
3.3 PACKAGE MECHANICAL DATA

Figure 18. 28-Plastic Dual In line Package, 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		4.8	0.086		0.189
A1	0.51		1.77	0.010		0.069
B	0.38		0.58	0.015		0.023
B1	0.97		1.52	0.055		0.065
C	0.2		0.3	0.008		0.009
D	35.06		36.22	1.400		1.425
D1	–	–	–	–	–	–
E			16.3			0.641
E1		12.9				0.508
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	3.18		4.44	1.25		0.174
e1		2.54			0.10	
Number of Pins						
N	28					

Figure 19. 28-Lead Small Outline Plastic, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	17.7		18.1	.6969		.7125
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	28					

3.4 ORDERING INFORMATION

Ordering Information Table

Sales Types	Memory Type	Temperature Range	Package
ST7291B1 ST7291M1	16K ROM	-0 to + 70°C	PDIP28 PSO28

ST7291 MICROCONTROLLER REFERENCES

Customer:.....
Address: .....
Contact: .....
Phone No: .....
Reference:.....

SGS-THOMSON Microelectronics references

Device ST7291

Package [ ] Plastic Dual in Line [ ] Plastic Small Output

Temperature Range 0 to 70°C

Software Development
[ ] Customer [ ] SGS-THOMSON [ ] External Laboratory

For marking one line with 11 characters maximum is possible

Special Marking [ ] No
[ ] Yes "_ _ _ _ _ _ _ _ _ _ _"
Letters, digits, ' . ', ' - ', ' / ' and spaces only

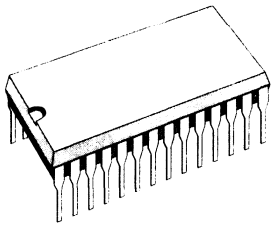
Signature .....

Date .....

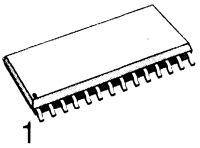
8-BIT HCMOS MCUs WITH EEPROM

PRELIMINARY DATA

- 2.5 to 5.5V supply operating range
- 4MHz Maximum Clock Frequency
- Fully static operation
- -25 to +85°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention Modes
- User ROM: 3328 bytes
  Data RAM: 128 bytes
  EEPROM: 128 bytes
- 28 pin Dual In Line and SO plastic packages
- 22 bidirectional I/O lines
- 6 lines programmable as interrupt wake-up inputs
- 16-bit timer with 1 input capture and 2 output compares
- Master Reset and power on reset
- Full Hardware Emulator
- User mask options:
  - internal clock for timer (÷ 2,÷ 4,÷ 8)
  - pinout for ICAP and OCMP1 signals
  - enable wake-up function on PORT C
  - open drain on PORT A
  - Watchdog enable/disable after Reset
  - Watchdog enable during WAIT mode
- 8-bit data manipulation
- 74 basic instructions
- 10 main addressing modes
- 8x8 unsigned multiply instruction
- true bit manipulation
- Complete development support on real time emulator with PC/DOS
- Full software package (Cross Assembler, debugger)



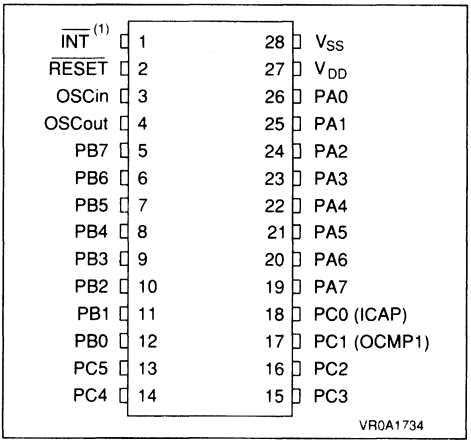
PDIP28



PSO28

(Ordering Information at the end of the datasheet)

Pin Configuration



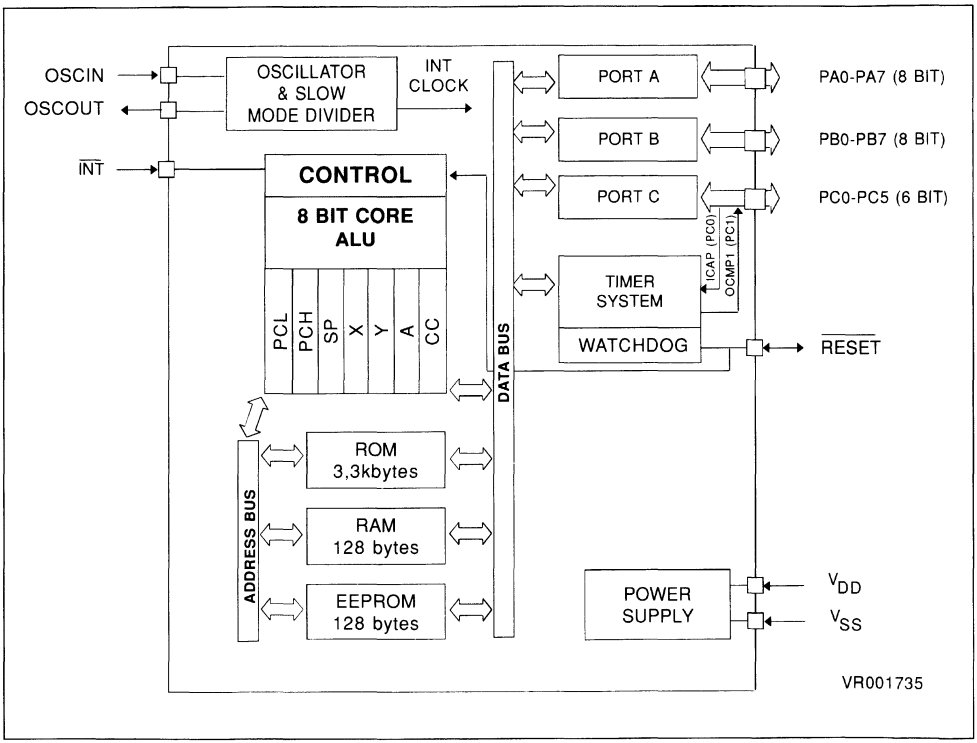
Note 1. This pin is also the VPP input for EPROM based devices

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST7293 is a HCMOS microcontroller unit (MCU) from the ST72 family. It is based around an industry standard 8 bit core and offers an enhanced instruction set. The processor runs with an external clock at 4 MHz with a 5V supply and 2MHz with a 3V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST7293 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST7293 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes an on-chip oscillator, CPU, ROM, RAM, EEPROM, I/O, and one timer with 1 input capture and 2 output compare systems.

Figure 1. ST7294 Block Diagram



1.2 PIN DESCRIPTION

V_{DD}. Single power supply voltage 2.5 to 5.5V.

V_{SS}. Ground

OSCin, OSCout. Oscillator input and output pins. These pins are to be connected to a parallel resonant crystal or ceramic resonator. An external clock source can also be input through OSCin.

$\overline{\text{RESET}}$. The active low input signal forces the initialization of the MCU. This event is the first priority non maskable interrupt. This pin is switched output low when the Watchdog has released. It could be used to reset external peripherals.

$\overline{\text{INT}}$ is the external interrupt signal. Software configuration allows four triggering modes.

ICAP (PC0). Input capture signal going to the TIMER system. This signal, according to a mask option, can be an ICAP pin or PC0 pin. When PC0 is defined as ICAP, the internal pull-up resistor is not connected.

OCMP1 (PC1). Output compare signal coming from the TIMER system. This output signal, according to a mask option, can be an OCMP1 pin(for output compare 1 of the timer) or PC1 pin. When PC1 is defined as OCMP1, the internal pull-up resistor is not connected.

PA0-PA7, PB0-PB7, PC0-PC5. These 22 lines are standard I/O lines, programmable as either input or output.

- PORT A. 8 Standard I/O lines, bit programmable, accessed through DDRA and DRA Registers. According to a mask option, each output can be defined as a standard push-pull output port or as an open drain output port.

- PORT B. 8 Standard I/O lines bit programmable accessed through DDRB and DRB Registers.

- PORT C. 6 Standard I/O lines accessed through DDRC and DRC Registers. According to a mask option, these 6 lines can become 6 falling edge sensitive interrupt lines all linked to a single interrupt vector or 6 standard input ports tied to Vdd through an internal pull-up resistor (250kΩ typical at V_{DD} = 3.5V).

PIN DESCRIPTION (Continued)

Table 1. ST7293 Pin Configuration

Name	Function	Description	Pin Assignment
$\overline{INT}$	I	Interrupt	1
$\overline{RESET}$	I/O	Reset	2
OSCin	I	Oscillator	3
OSCout	O	Oscillator	4
PB7	I/O	Standard Port (bit programmable)	5
PB6	I/O	Standard Port (bit programmable)	6
PB5	I/O	Standard Port (bit programmable)	7
PB4	I/O	Standard Port (bit programmable)	8
PB3	I/O	Standard Port (bit programmable)	9
PB2	I/O	Standard Port (bit programmable)	10
PB1	I/O	Standard Port (bit programmable)	11
PB0	I/O	Standard Port (bit programmable)	12
PC5	I/O	Standard Port (falling edge interrupt line)	13
PC4	I/O	Standard Port (falling edge interrupt line)	14
PC3	I/O	Standard Port (falling edge interrupt line)	15
PC2	I/O	Standard Port (falling edge interrupt line)	16
PC1 (OCMP1)	I/O	Standard Port (falling edge interrupt line)	17
PC0 (ICAP)	I/O	Standard Port (falling edge interrupt line)	18
PA7	I/O	Standard Port (bit programmable)	19
PA6	I/O	Standard Port (bit programmable)	20
PA5	I/O	Standard Port (bit programmable)	21
PA4	I/O	Standard Port (bit programmable)	22
PA3	I/O	Standard Port (bit programmable)	23
PA2	I/O	Standard Port (bit programmable)	24
PA1	I/O	Standard Port (bit programmable)	25
PA0	I/O	Standard Port (bit programmable)	26
V_{DD}		Power Supply	27
V_{SS}		Ground	28

1.3 CENTRAL PROCESSING UNIT

1.3.1 Introduction

The CPU has a full 8-bit architecture. Six internal registers allow efficient 8-bit data manipulations. The CPU is able to execute 74 basic instructions. It features 10 main addressing modes. It is able to address 8192 bytes of memory and registers with its program counter.

1.3.2 CPU Registers

The 6 CPU registers are shown in the programming model in Figure 2. Following an interrupt, the registers are pushed onto the stack in the order shown in Figure 3. They are popped from stack in the reverse order. The Y register is not affected by these automatic procedures. The interrupt routine must therefore handle it, if needed, through the POP and PUSH instructions.

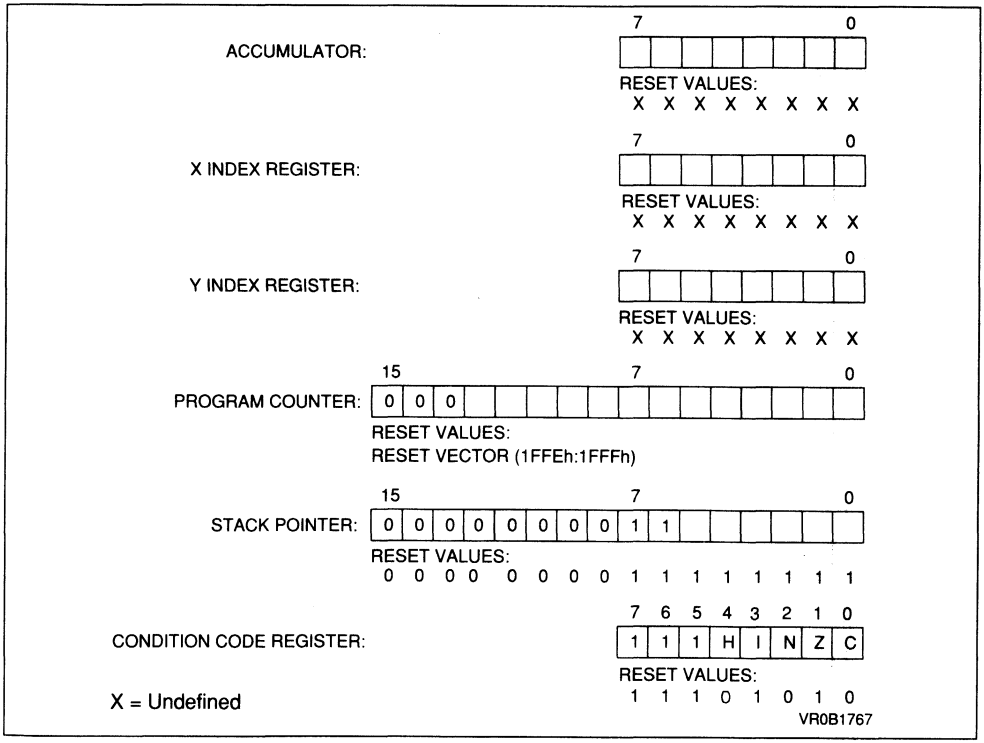
Accumulator (A). The accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations as well as data manipulations.

Index Registers (X and Y). These 8-bit registers are used to create effective addresses or as temporary storage area for data manipulations. The cross assembler generates a PRECEDE instruction (PRE) to indicate that the following instruction refers to the Y register. The Y register is never automatically stacked. Interrupt routines must push or pop it by using the POP and PUSH instructions.

Program Counter (PC). The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. In the ST7294, only the 13 low order bits are used, bits 13, 14 and 15 are forced to "0".

Stack Pointer (SP). The stack pointer is a 16-bit register. The 6 least significant bits contain the address of the next free location of the stack. The 10 most significant bits are forced as indicated in Figure 2. They are reserved for future extension of ST72 family.

Figure 2. Programming Model



CENTRAL PROCESSING UNIT (Continued)

The stack is used to save the CPU context on subroutines calls or interrupts. The user can also directly use it through the POP and PUSH instructions.

After a MCU reset or after the reset stack pointer instruction (RSP), the stack pointer is set to its upper value (0FFh). It is then decremented after data has been pushed onto the stack and incremented after data is popped from the stack. When the lower limit is exceeded, the stack pointer wraps around to the stack upper limit. The previously stored information is then over written and therefore lost.

A subroutine call occupies two locations and an interrupt five locations.

1.3.3 Condition Code Register (CC).

The condition code register is a 5 bit register which indicates the result of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. The following paragraphs describe each bit.

Half carry bit (H). The H bit is set to 1 when a carry occurs between the bits 3 and 4 of the ALU during an ADD or ACC instruction. The H bit is useful in BCD arithmetic subroutines.

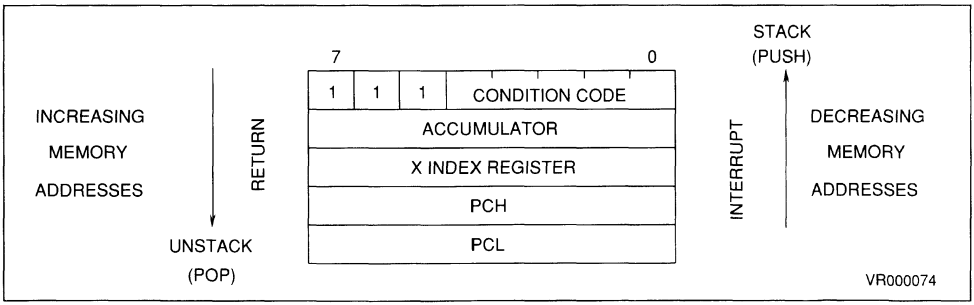
Interrupt mask (I). When the I bit is set to 1, all interrupts are disabled. Clearing this bit enables them. Interrupts requested while I is set are latched and can be processed when I is cleared (only one interrupt request per interrupt enable flag can be latched).

Negative (N). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is negative (i.e. the most significant bit is a logic 1).

Zero (Z). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

Carry/Borrow (C). When set, C indicates that a carry or borrow out of the ALU occurred during the last arithmetic operation. This bit is also affected during bit test, branch, shift and rotate instructions.

Figure 3. Stacking Order



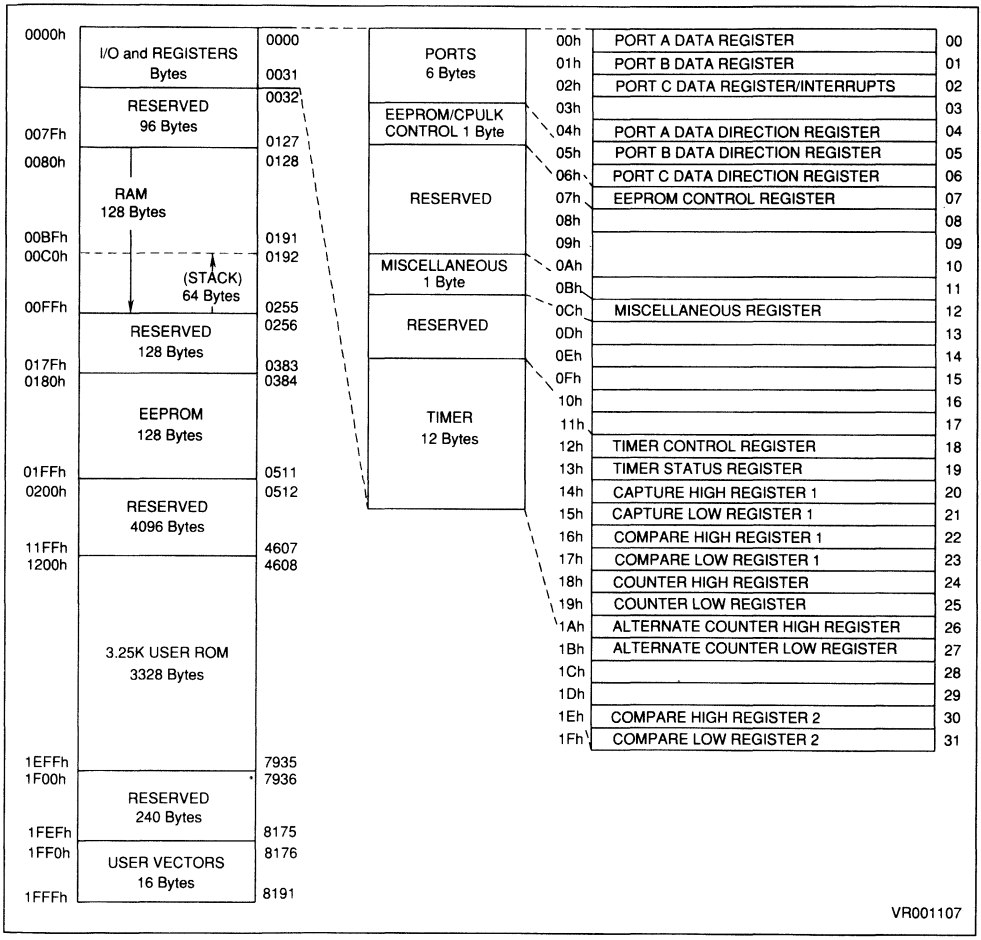
1.4 MEMORY MAP

As shown in Figure 4, the MCU is capable of addressing 8192 bytes of memory and I/O registers. In the ST7293 3604 of these bytes are user accessible.

The locations consist of 32 bytes of I/O registers (only 20 are used), 128 bytes of RAM, 128 bytes of EEPROM and 3.25Kbytes of user ROM. The RAM space includes 64 bytes for the stack from 0FFh to 0C0h. Programs that only use a small part of the allocated stack locations for interrupts and/or subroutine stacking purpose can use the remaining bytes as standard RAM locations.

The highest address bytes contains the user defined reset and interrupt vectors.

Figure 4. Memory Map



1.5 WATCHDOG SYSTEM

The watchdog system consists in a divider-by-8 counter and a fixed divide-by-1024 prescaler. It is controlled through bit WDOG of the Miscellaneous Register. Two mask options are provided.

The watchdog enable mode mask option selects the state of the watchdog system after an external or a power-on reset. In the "programmable enable" option, a reset causes the watchdog to be disabled and the counter to be forced to zero. When the watchdog is configured with the "programmable enable" option, the watchdog system is enabled by setting the WDOG bit of the Miscellaneous Register (0Ch). Only an external or a power-on reset can clear WDOG and disable the watchdog system.

Whatever the option, when the watchdog counter is enabled, it is driven by the CPU clock through the divide-by-1024 prescaler (i.e. the counter clock period is 1024 CPU clock cycles). It is reset to zero by writing WDOG at 1. A system reset is generated if the counter reaches it maximum count (8). To avoid a system reset, the software must therefore reset the counter at least after a time tdog from the last clear or from the time the watchdog system has been enabled.

Care has to be taken when enabling the counter ("programmable enable" option only). The prescaler is actually in an unknown state at the time WDOG is set. The first rising edge can thus be sent to the watchdog counter after a time comprised between 0 and 1024 CPU clock cycles. In this mode, the first reset of the watchdog counter should therefore not occur later than 6x1024 CPU clock cycles after it has been enabled.

The system reset is generated by pulling down the RESET pin for at least one and a half CPU clock cycle. The state of the RESET pin is re-entered, thus causing an external reset to be issued.

The WATCHDOG DURING WAIT mask option allows to determine the watchdog function during the WAIT low power mode. In the "active during WAIT" option, the watchdog is kept active, thus able to reset the MCU if it remains in WAIT mode longer than the watchdog timeout period. In the "suspended during WAIT" option, it suspends operation during the WAIT mode and resets its counter. It will then resume operation when exiting the WAIT mode.

The HALT mode is inhibited when the watchdog system is enabled. However if a HALT instruction is executed while it is enabled, a watchdog reset is immediately generated.

1.6 MISCELLANEOUS REGISTER

Miscellaneous Register (000Ch)
Read/Write

Reset Value: 0001 000 (10h)

This register is a various 8-Bit register where only 4bits are used for interrupt, slow mode and Watchdog purposes.

7							0
—	INTP	INTN	—	—	—	SM	WDOG

b7, b4-b2 = Unused

b6 = **INTP**: *External Interrupt Positive* allows to select the INT line triggering mode in conjunction with INTN. It can only be modified when the I bit of the CCR is set.

b5 = **ININ** :*External Interrupt Negative* allows to select the INT line triggering mode in conjunction with INTP. It can only be modified when the I bit of the CCR is set.

b1 = **SM**: *Slow Mode*. Setting this bit to "1" enables Slow Mode, thus reducing power consumption. In this mode, an extra divider by 16 is added in the clock circuitry.

b0 = **WDOG**: *Watchdog System*. Whatever the WATCHDOG ENABLE MODE mask option, the watchdog counter is reset when WDOG is written at 1. When the MCU is configured with the "programmable enable" option, the WDOG bit is low after a reset. It must be set to enable the watchdog system. Only a reset can clear WDOG.

1.7 CLOCK SYSTEM

1.7.1 General Description

The MCU accepts either a Crystal/Ceramic resonator or an external clock to provide the internal oscillator. The internal clock (fop) is derived by a divide-by-2 from the external oscillator frequency (fosc).

The slow mode function allows under software control to further slow down the internal clock, thus reducing power consumption. This feature is particular useful in WAIT mode.

The slow mode is entered by setting the SM bit in the Miscellaneous Register (0Ch). This mode affects all functions, including timer and EEPROM. The slow mode is exited by clearing SM or by entering the STOP mode.

Crystal . The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for fosc. The circuit shown on Figure 5 is recommended when using a crystal. The table lists the recommended capacitance and feedback resistance values.

Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and startup stabilization time.

Ceramic Resonator. A ceramic resonator may be used in place of the crystal in low cost applications. The circuit on Figure 5 is recommended when using a ceramic resonator. The table lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

External Clock. An external clock should be applied to the OSCin input with the OSCout pin not connected, as shown on Figure 6. The t_{OXOV} and t_{ILCH} specifications do not apply when using an external clock input. The equivalent specification of the external clock source should be used instead of t_{OXOV} or t_{ILCH}.

Figure 5. Crystal/Ceramic Resonator

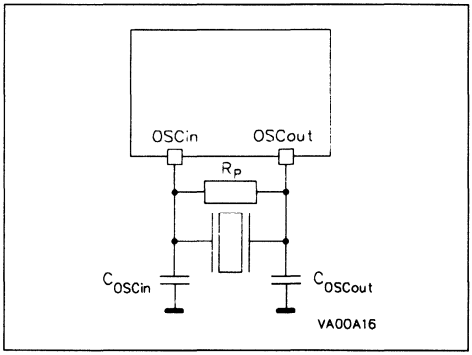
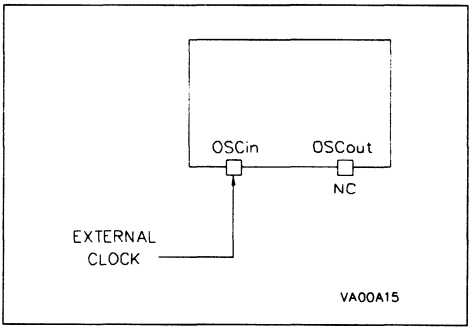
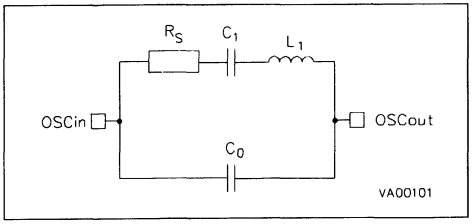


Figure 6. External Clock Source Connections



CLOCK SYSTEM (Continued)

Figure 7. Equivalent Crystal Circuit



Recommended Settings for Crystal

	2MHz	4MHz	Unit
R_{SMAX}	400	75	Ω
C_0	5	7	pF
C_1	0.008	0.012	pF
C_{OSCin}	15-40	15-30	pF
C_{OSCout}	15-30	15-25	pF
R_P	10	10	MΩ
Q	30	40	10^3

Recommended Settings for Ceramic Resonator

	2-4MHz	Unit
R_{SMAX}	10	Ω
C_0	40	pF
C_1	4.3	pF
C_{OSCin}	30	pF
C_{OSCout}	30	pF
R_P	1-10	MΩ
Q	1250	

1.8 RESETS AND INTERRUPTS

Resets are used to provide an orderly software startup procedure or to quit low power modes.

Two reset modes are provided: a power-on reset and an external reset at pin RESET. The watchdog reset is considered as an external one though the watchdog system generates a MCU reset by pulling down the RESET pin.

A summary of the effects of both reset modes on the different sections of the MCU is given in the following Table. For further information, please refer to the part describing the particular section.

1.8.1 External Reset

The external reset is an active low input signal applied to the RESET pin of the MCU.

As shown in Figure 8, the RESET signal must stay low for a minimum of one and a half CPU clock cycles. A reset causes the reset vector to be fetched at addresses 01FFEh and 01FFFh in order to be loaded into the PC.

The external reset is used by the watchdog system to reset the MCU. When active, the power-on reset circuitry pulls down the RESET pin. In both cases, the RESET pin can be used as an output to reset other devices. However, the pull down circuitry features a current limitation to allow the connection of any input signal, including from an RC type circuit.

An internal Schmitt trigger at pin RESET improves noise immunity.

1.8.2 Power-on Reset (POR)

The power-on reset (POR) is generated upon detection of a positive transition on V_{DD} (refer to Figure 8). It causes the reset vector to be fetched at addresses 01FFEh and 01FFFh in order to be loaded into the PC.

An internal circuitry provides a 4096 CPU clock cycle delay from the time the oscillator becomes active. At the end of the power-on reset, the MCU can be maintained in the reset condition by the external reset. The RESET pin can therefore be used to ensure V_{DD} has risen to a point where the MCU can properly operate before running the MCU program.

RESET AND INTERRUPTS (Continued)

During the POR, the RESET pin is pulled low, thus permitting the MCU to reset other devices.

The power-on reset is strictly used for power up conditions and should not be used to detect any drop in the power supply voltage. There is no provision for a power-down reset.

1.8.3 Interrupts

The ST7293 may be interrupted by one of four different methods: the three maskable hardware interrupts (INT, PORT C, or TIMER) and the non-maskable software interrupt (TRAP). The Interrupt processing flowchart is shown in Figure 9. The maskable interrupts must be enabled in order to be serviced. However, disabled interrupts can be latched and processed when they are enabled. When an interrupt has to be serviced, the PC, X, A and CC registers are saved into the stack and the interrupt mask (I bit of the Condition Code Register) is set to prevent additional interrupts. The Y register is not automatically saved. The stack order is shown on Figure 3.

The PC is then loaded with the interrupt vector of the interrupt to service and the interrupt service routine runs (refer to Table 3 for vector addresses).

It should finish by the IRET instruction which causes the contents of the registers to be recovered from the stack and normal processing to resume. Note that the I bit is then cleared if and only if the corresponding bit stored in the stack is zero.

Though many interrupts can be simultaneously pending, a priority order is defined (see Table 4). The RESET pin has the highest priority. Then, if the I bit is low, the decreasing priority order is TRAP, INT, timer input capture, timer output compare, timer overflow and PORT C. If the I bit is set, TRAP is the only enabled interrupt.

Interrupts allow the processor to leave low power modes. Refer to LOW POWER MODES for further information.

Software Interrupt. The software interrupt is the TRAP executable instruction. The interrupt is recognized when the TRAP instruction is executed, regardless to the I bit state. When the interrupt is recognized, it is serviced according to the flowchart on Figure 9.

External Interrupt. The external interrupt is generated through the INT pin. The interrupt is enabled if the I bit of the CCR is cleared.

Table 2. List of sections affected by RESET, WAIT and HALT

Section	RESET	POR	WAIT	HALT
Timer Prescaler reset to zero	X	X	-	-
Timer Counter set to FFFCh	X	X	-	-
All Timer enable bit set to 0 (disable)	X	X	-	-
Data Direction Regfisters set to 0 (as Inputs)	X	X	-	-
Set Stack Pointer to 00FFh	X	X	-	-
Force Internal Address Bus to restart vector 1FFEh, 1FFFh	X	X	-	-
Set Interrupt Mask Bit (I-Bit, CCR) to 1 (Interrupt Disable)	X	X	-	-
Set Interrupt Mask Bit (I-Bit, CCR) to 0 (Interrupt Enable)	-	-	X	X
Reset HALT Latch	X	X	-	-
Reset INT Latch	X	X	-	-
Reset WAIT Latch	X	X	-	-
Disable fop Clock (for 4096 cycles)	-	X	-	X
Set CPU Clock to 0	-	X	X	X
Set Timer Clock to 0	-	X	-	X
SM-Bit cleared	X	X	-	X
Watchdog counter reset	X	X	-	X
Watchdog WDOG-BIT reset	X	X	-	X
EEPROMs control bits reset	X	X	-	-

RESET AND INTERRUPTS (Continued)

The INTN and INTP bits of the Miscellaneous Register (0Ch) allow selection of the interrupt triggering mode among the 4 available ones. Refer to Table 3 for the triggering mode coding.

In order to avoid conflicts and spurious interrupts, the external interrupt options can only be changed when the I bit is set. Any attempt to change the options while I is reset fails. When the options are changed any pending interrupt is lost.

When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution. It is then processed according to the flowchart on Figure 9.

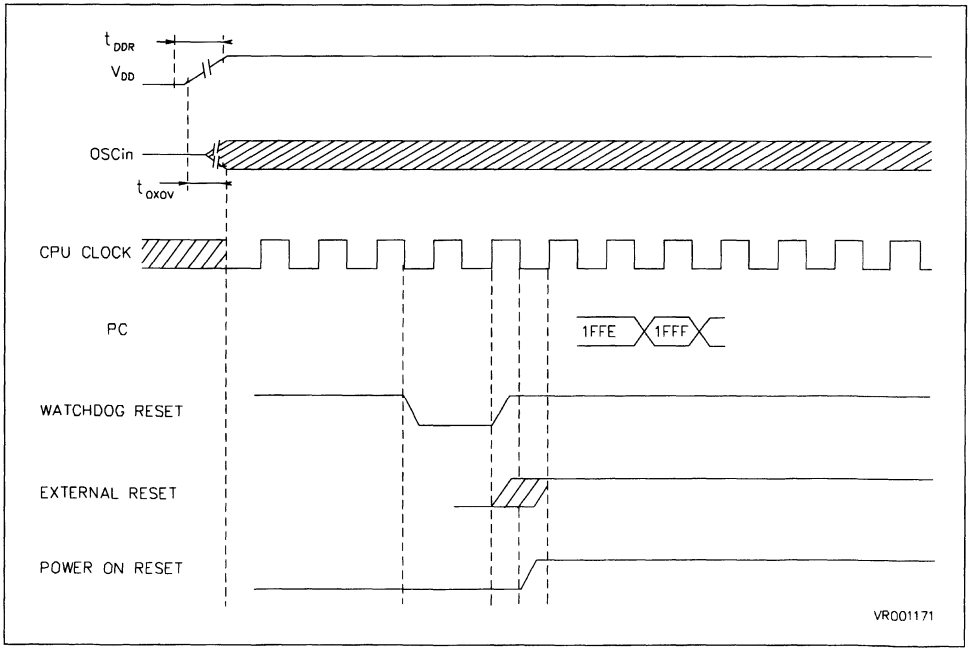
If the interrupt is disabled (I high), the triggering edge of the INT line is internally latched and the interrupt remains pending to be processed as soon as the interrupt is enabled (the low level sensitive interrupt is not latched and can therefore not remain pending). This internal latch is cleared in the first part of the service routine. Therefore, one, and one only, external interrupt can be latched and serviced as soon as enabled.

Figure 10 shows the mode timing diagram for the interrupt line. Two methods are described. The first method shows single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an IRET instruction occurs).

The second configuration shows several interrupt lines "wire-ORed" to form the interrupts at the processor. Thus, if after servicing one interrupt the interrupt line remains low, then the next interrupt is recognized.

PORTC Interrupt. The PORTC Interrupt can be generated on the falling edge of one pin PC0-PC5 if it is defined as an interrrupt source. When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution. It is then processed according to the flowchart on Figure 9.

Figure 8. Reset Timing Diagram

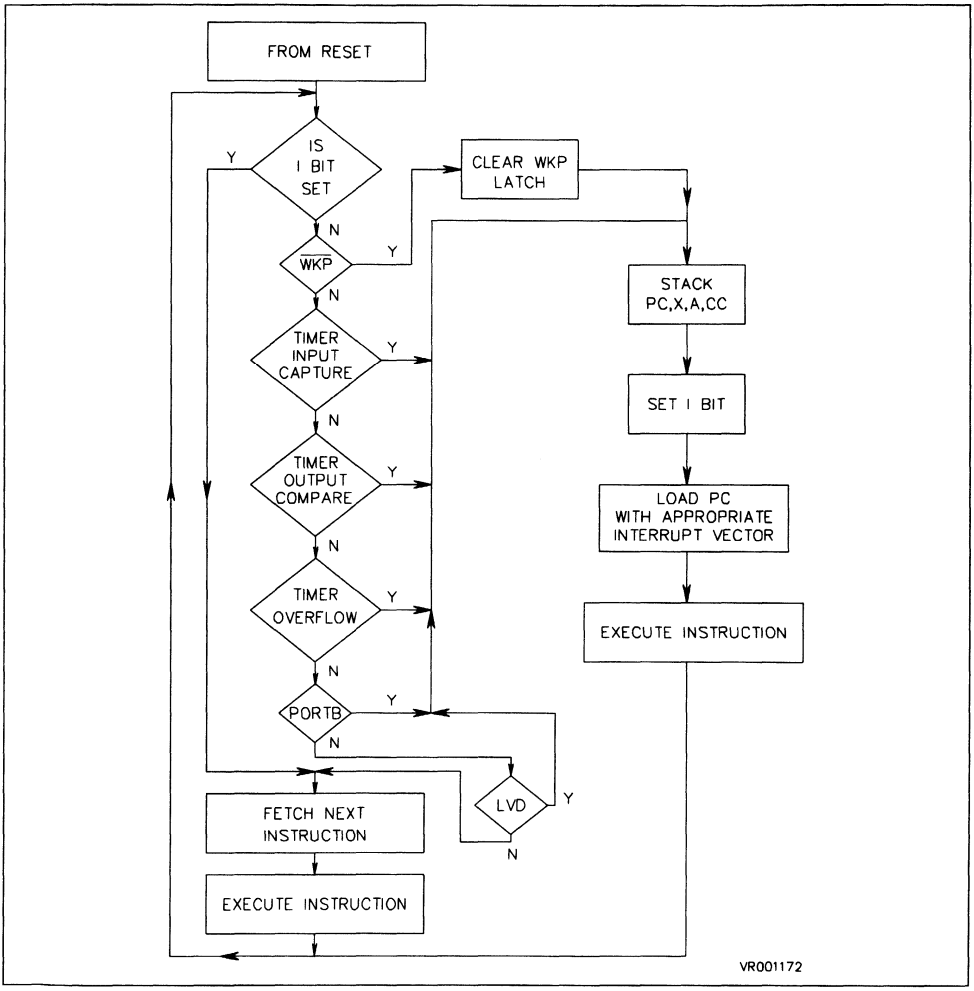


RESET AND INTERRUPTS (Continued)

Table 3. External Interrupt Options

INTP	INTN	External Interrupt Options
0	0	Negative edge and Low level sensitive
0	1	Negative edge only
1	0	Positive edge only
1	1	Positive and negative edge sensitive

Figure 9. Interrupt Processing Flow-Chart



RESET AND INTERRUPTS (Continued)

If the interrupt is disabled (I high), the triggering edge of the wake-up interrupt sources logical-OR is internally latched and the interrupt remains pending to be processed as soon as the interrupt is enabled. This internal latch is cleared in the first part of the service routine. Therefore, one and one only external interrupt can be latched and serviced as soon as possible.

Timer Interrupt. Four different timer interrupt flags are able to cause a timer interrupt when they are active if both the I bit of the CCR is reset and if the corresponding enable bit is set. If either of these conditions is false, the interrupt is latched and thus remains pending.

The interrupt flags are located in the Timer Status Register (0013h). The Enable bit are in the Timer Control Register (0012h).

When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution. it is then serviced according to the flowchart on Figure 9. Software in the timer service routine must determine the priority and cause of the timer interrupt by examining the interrupt flags and the status bits located in the TSR.

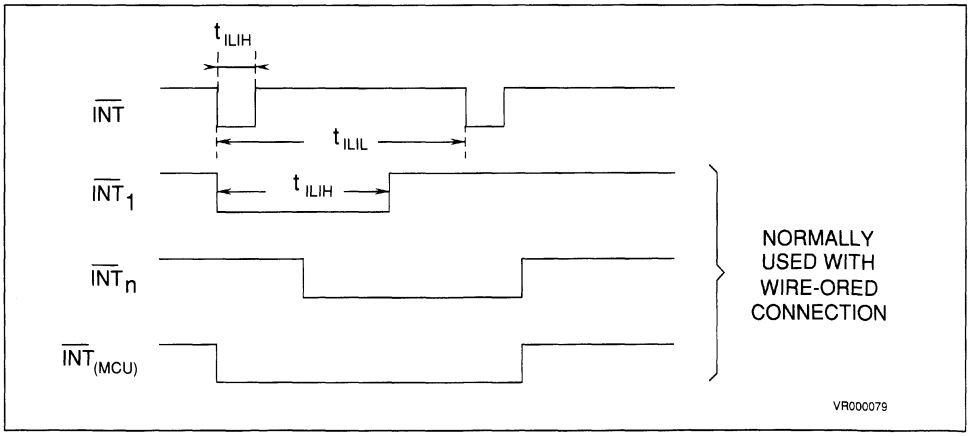
The general sequence for clearing an interrupt is an access to the status register while the flag is set followed by a read or write of an associated register. Note that the clearing sequence resets the internal latch. A pending interrupt (i.e. waiting for being enabled) will therefore be lost if the clear sequence is executed.

Refer to 16 BIT TIMER for further information.

Table 4. Interrupt and Reset priorities

Vector Address	Interrupt Source	Masked by	Priority
1FFEh,1FFFh	RESET and POWER-ON (POR)	none	Highest
1FFCh,1FFDh	SOFTWARE Interrupt (TRAP)	none	
1FFAh,1FFBh	EXTERNAL Interrupt (INT)	I-Bit	
1FF8h,1FF9h	TIMER INPUT Capture	I-Bit	
1FF6h,1FF7h	TIMER OUTPUT Compares (1 and 2)	I-Bit	
1FF4h,1FF5h	TIMER OVERFLOW	I-Bit	
1FF2h,1FF3h	Reserved	I-Bit	
1FF0h,1FF1h	PORTC Wake-up	I-Bit	Lowest

Figure 10. Timing Diagram for Interrupt Line



1.9 LOW POWER MODES

Table 2 gives a list of the different sections affected by the low power modes. For detailed information on a particular devices, please refer to the corresponding parts.

HALT Mode. The HALT mode is the MCU lowest power consumption mode. The HALT mode is entered by executing the HALT instruction. The internal oscillator is then turned off, causing all internal processing to be stopped, including the operation of the on-chip peripherals. The HALT mode cannot be used when the watchdog is enabled, if the HALT instruction is executed while the watchdog system is enabled, a watchdog reset is generated thus resetting the entire MCU.

When entering the HALT mode, the I bit in the Condition Code Register and the SM bit in the Miscellaneous Register are cleared. Thus, the external interrupts are allowed and the MCU is placed at its nominal speed (see CLOCK SYSTEM). All other registers and memory remain unaltered and all I/O lines remain unchanged.

The MCU can exit the HALT mode upon reception of either an external interrupt or PORTC or a power-on or external reset. The oscillator is then turned on and a stabilization time is provided before releasing CPU operation. The stabilization time is 4096 CPU clock cycles.

After the start up delay, the CPU continues operation by servicing the interrupt which wakes it up or by fetching the reset vector if a reset wakes it up.

WAIT Mode. This mode is a low power consumption mode, but the power consumption is higher than in the HALT mode. The consumption can be further reduced by entering the slow mode.

The WFI instruction places the MCU in the WAIT mode.

In the WAIT mode, the internal clock remains active but all CPU processing is stopped; however, the programmable timer remains in his previous state. The watchdog can either be active or not according to the WATCHDOG DURING WAIT mask option.

During the WAIT mode, the I bit in the condition code register is cleared to enable all interrupts.

All other registers and memory remain unaltered and all parallel I/O lines remain unchanged.

An interrupt or a reset causes the MCU to exit the WAIT mode. An interrupt while the MCU is in the WAIT mode causes the corresponding interrupt vector to be fetched, the interrupt routine to be executed and normal processing to resume. A reset causes the program counter to fetch the reset vector and processing starts as for a normal reset.

DATA RETENTION Mode. The contents of RAM and CPU registers are retained at supply voltage as low as 2.0 volts. This is referred to as the data retention mode, where the data is held, but the device is not guaranteed to operate.

LOW POWER MODES (Continued)

Figure 11. HALT Function Flow Chart

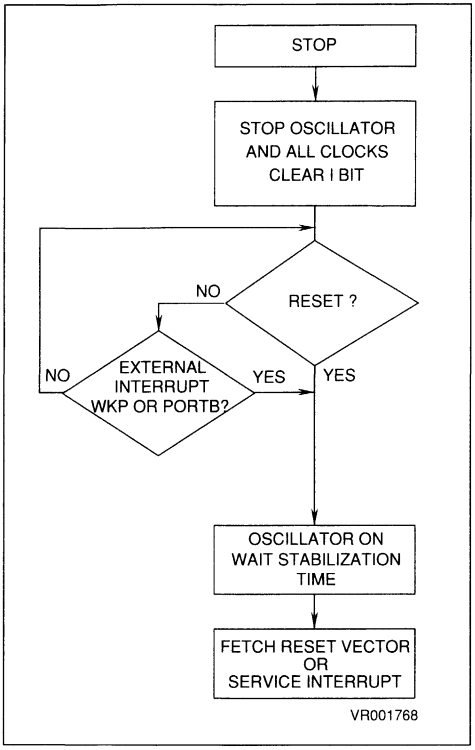
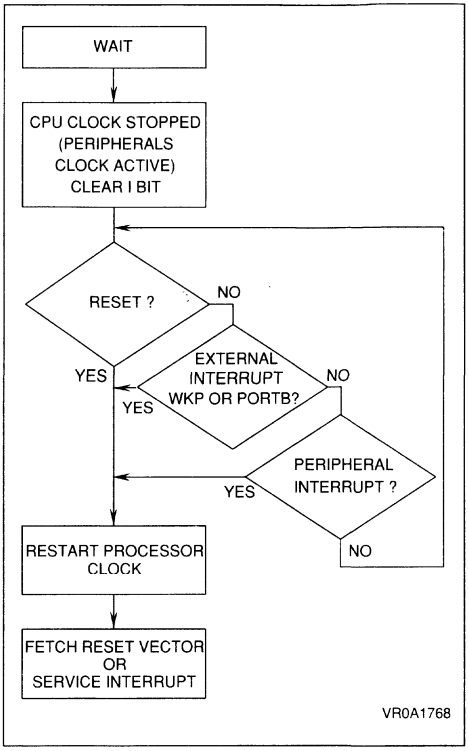


Figure 12. WAIT Flow Chart



1.10 ORDERING INFORMATION

Ordering Information

Sales Types	Memory Type	Temperature Range	Package
ST7293B1 ST7293M1	3.3K ROM	-0 to + 70°C	PDIP28 PSO28
ST7293B8 ST7293M8	3.3K ROM	-25 to + 85°C	PDIP28 PSO28

ST7293 MICROCONTROLLER OPTION LIST

Customer: .....
Address: .....
Contact: .....
Phone No: .....
Reference: .....

SGS-THOMSON Microelectronics references

Package	[ ] Plastic Dual in Line	[ ] Plastic Small Outline
Temperature Range	[ ] 0 to 70°C	[ ] -25 to 85°C
Software Development	[ ] Customer	[ ] SGS-THOMSON
	[ ] External Laboratory	

For marking one line with 11 characters maximum is possible
Special Marking [ ] (y/n) "_ _ _ _ _ _ _ _ _ _ _" Letters, digits, ' . ', ' - ', ' / ' and spaces only

OPTION LIST:

TIMER CLOCK	[ ] STANDARD ($f_{OP}/4$)	
	[ ] FAST ($f_{OP}/2$)	
	[ ] SLOW ($f_{OP}/8$)	
Watchdog ENABLE MODE	[ ] Software Enable	[ ] Auto Enable
Watchdog during WAIT	[ ] Active during WAIT mode	[ ] Suspend during WAIT mode
Enable Wake-up on PORTC	[ ] PORTC 6-bit I/O PORT	
	[ ] PORTC interrupt Wake-up inputs	
Pinout for ICAP (PC0)	[ ] ICAP is bonded on pin 18	
	[ ] PC0 is bonded on pin 18	
Pinout for OCMP1 (PC1)	[ ] OCMP1 is bonded on pin 17	
	[ ] PC1 is bonded on pin 17	
PORT A Outputs	[ ] Standard push-pull output PORT	
	[ ] Open Drain output PORT	

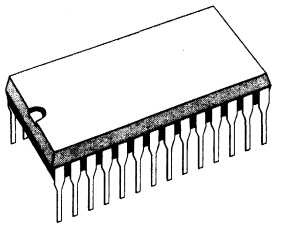
Signature .....

Date .....

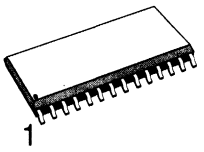
8-BIT HCMOS MCUs WITH EEPROM

PRELIMINARY DATA

- 2.5 to 5.5V supply operating range
- 4MHz Maximum Clock Frequency
- Fully static operation
- -25 to +85°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention Modes
- User ROM: 6144 bytes
  Data RAM: 224 bytes
  EEPROM: 256 bytes
- 28 pin Dual In Line and SO plastic packages
- 22 bidirectional I/O lines
- 6 lines programmable as interrupt wake-up inputs
- 16-bit timer with 1 input capture and 2 output compares
- 2V RAM retention mode
- Master Reset and power on reset
- Full Hardware Emulator
- User mask options:
  - internal clock for timer (÷ 2,÷ 4,÷ 8)
  - pinout for ICAP and OCMP1 signals
  - enable wake-up function on PORT C
  - open drain on PORT A
  - pull-up on PORT A and PORT B
  - Watchdog enable/disable after Reset
  - Watchdog enable during WAIT mode
- 8-bit data manipulation
- 74 basic instructions
- 10 main addressing modes
- 8x8 unsigned multiply instruction
- true bit manipulation
- Complete development support on real time emulator with PC/DOS
- Full software package (Cross Assembler, debugger)



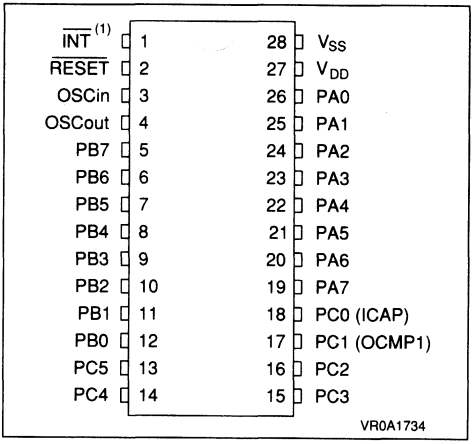
PDIP28



PSO28

(Ordering Information at the end of the datasheet)

Pin Configuration



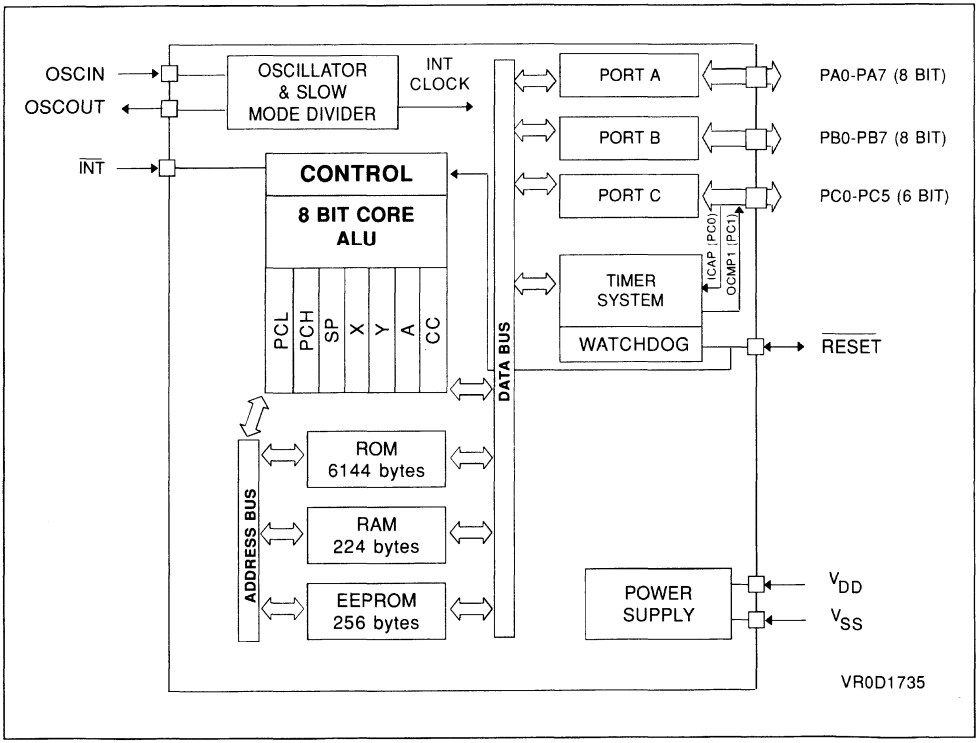
Note 1. This pin is also the VPP input for EPROM based devices

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST7294 is a HCMOS microcontroller unit (MCU) from the ST72 family. It is based around an industry standard 8 bit core and offers an enhanced instruction set. The processor runs with an external clock at 4 MHz with a 5V supply and 2MHz with a 3V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST7294 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST7294 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes an on-chip oscillator, CPU, ROM, RAM, EEPROM, I/O, and one timer with 1 input capture and 2 output compare systems.

Figure 1. ST7294 Block Diagram



1.2 PIN DESCRIPTION

V_{DD}. Single power supply voltage 2.5 to 5.5V.

V_{SS}. Ground

OSCin, OSCout. Oscillator input and output pins. These pins are to be connected to a parallel resonant crystal or ceramic resonator. An external clock source can also be input through OSCin.

$\overline{\text{RESET}}$. The active low input signal forces the initialization of the MCU. This event is the first priority non maskable interrupt. This pin is switched output low when the Watchdog has released. It could be used to reset external peripherals.

$\overline{\text{INT}}$ is the external interrupt signal. Software configuration allows four triggering modes.

ICAP (PC0). Input capture signal going to the TIMER system. This signal, according to a mask option, can be an ICAP pin or PC0 pin. When PC0 is defined as ICAP, the internal pull-up resistor is not connected.

OCMP1 (PC1). Output compare signal coming from the TIMER system. This output signal, according to a mask option, can be an OCMP1 pin(for output compare 1 of the timer) or PC1 pin. When PC1 is defined as OCMP1, the internal pull-up resistor is not connected.

PA0-PA7, PB0-PB7, PC0-PC5. These 22 lines are standard I/O lines, programmable as either input or output.

- PORT A. 8 Standard I/O lines, bit programmable, accessed through DDRA and DRA Registers. According to a mask option, each output can be defined as a standard push-pull output port or as an open drain output port. According to another mask option, a pull-up resistor (250kΩ typical at V_{DD}=3.5V) can be added on each line when it is defined as an input.

- PORT B. 8 Standard I/O lines bit programmable accessed through DDRB and DRB Registers. According to a mask option, a pull-up resistor (250kΩ typical at V_{DD}=3.5V) can be added on each line when it is defined as an input.

- PORT C. 6 Standard I/O lines accessed through DDRC and DRC Registers. According to a mask option, these 6 lines can become 6 falling edge sensitive interrupt lines all linked to a single interrupt vector or 6 standard input ports tied to Vdd through an internal pull-up resistor (250kΩ typical at V_{DD} = 3.5V). These negative edge sensitive interrupt lines can wake-up the ST7294 from WAIT or HALT mode. This feature allows to build low power applications when the ST7294 can be waken-up from keyboard push.

PIN DESCRIPTION (Continued)

Table 1. ST7294 Pin Configuration

Name	Function	Description	Pin Assignment
$\overline{INT}$	I	Interrupt	1
$\overline{RESET}$	I/O	Reset	2
OSCin	I	Oscillator	3
OSCout	O	Oscillator	4
PB7	I/O	Standard Port (bit programmable)	5
PB6	I/O	Standard Port (bit programmable)	6
PB5	I/O	Standard Port (bit programmable)	7
PB4	I/O	Standard Port (bit programmable)	8
PB3	I/O	Standard Port (bit programmable)	9
PB2	I/O	Standard Port (bit programmable)	10
PB1	I/O	Standard Port (bit programmable)	11
PB0	I/O	Standard Port (bit programmable)	12
PC5	I/O	Standard Port (falling edge interrupt line)	13
PC4	I/O	Standard Port (falling edge interrupt line)	14
PC3	I/O	Standard Port (falling edge interrupt line)	15
PC2	I/O	Standard Port (falling edge interrupt line)	16
PC1 (OCMP1)	I/O	Standard Port (falling edge interrupt line)	17
PC0 (ICAP)	I/O	Standard Port (falling edge interrupt line)	18
PA7	I/O	Standard Port (bit programmable)	19
PA6	I/O	Standard Port (bit programmable)	20
PA5	I/O	Standard Port (bit programmable)	21
PA4	I/O	Standard Port (bit programmable)	22
PA3	I/O	Standard Port (bit programmable)	23
PA2	I/O	Standard Port (bit programmable)	24
PA1	I/O	Standard Port (bit programmable)	25
PA0	I/O	Standard Port (bit programmable)	26
V_{DD}		Power Supply	27
V_{SS}		Ground	28

1.3 CENTRAL PROCESSING UNIT

1.3.1 Introduction

The CPU has a full 8-bit architecture. Six internal registers allow efficient 8-bit data manipulations. The CPU is able to execute 74 basic instructions. It features 10 main addressing modes. It is able to address 8192 bytes of memory and registers with its program counter.

1.3.2 CPU Registers

The 6 CPU registers are shown in the programming model in Figure 2. Following an interrupt, the registers are pushed onto the stack in the order shown in Figure 3. They are popped from stack in the reverse order. The Y register is not affected by these automatic procedures. The interrupt routine must therefore handle it, if needed, through the POP and PUSH instructions.

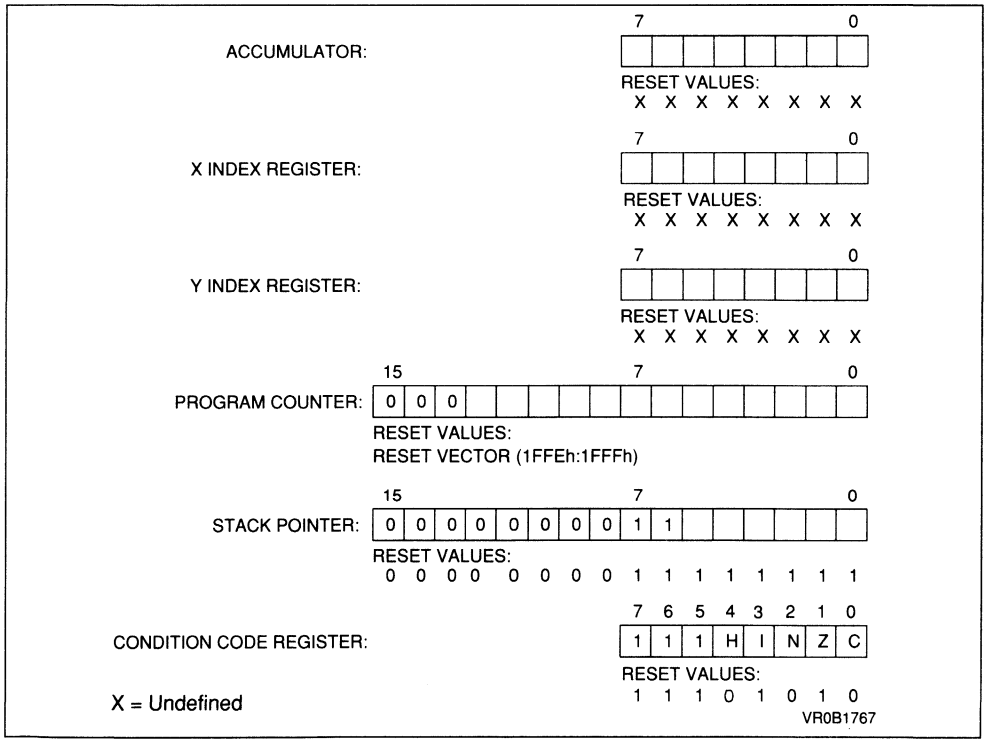
Accumulator (A). The accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations as well as data manipulations.

Index Registers (X and Y). These 8-bit registers are used to create effective addresses or as temporary storage area for data manipulations. The cross assembler generates a PRECEDE instruction (PRE) to indicate that the following instruction refers to the Y register. The Y register is never automatically stacked. Interrupt routines must push or pop it by using the POP and PUSH instructions.

Program Counter (PC). The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. In the ST7294, only the 13 low order bits are used, bits 13, 14 and 15 are forced to "0".

Stack Pointer (SP). The stack pointer is a 16-bit register. The 6 least significant bits contain the address of the next free location of the stack. The 10 most significant bits are forced as indicated in Figure 2. They are reserved for future extension of ST72 family.

Figure 2. Programming Model



CENTRAL PROCESSING UNIT (Continued)

The stack is used to save the CPU context on subroutines calls or interrupts. The user can also directly use it through the POP and PUSH instructions.

After a MCU reset or after the reset stack pointer instruction (RSP), the stack pointer is set to its upper value (0FFh). It is then decremented after data has been pushed onto the stack and incremented after data is popped from the stack. When the lower limit is exceeded, the stack pointer wraps around to the stack upper limit. The previously stored information is then over written and therefore lost.

A subroutine call occupies two locations and an interrupt five locations.

1.3.3 Condition Code Register (CC).

The condition code register is a 5 bit register which indicates the result of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. The following paragraphs describe each bit.

Half carry bit (H). The H bit is set to 1 when a carry occurs between the bits 3 and 4 of the ALU during an ADD or ACC instruction. The H bit is useful in BCD arithmetic subroutines.

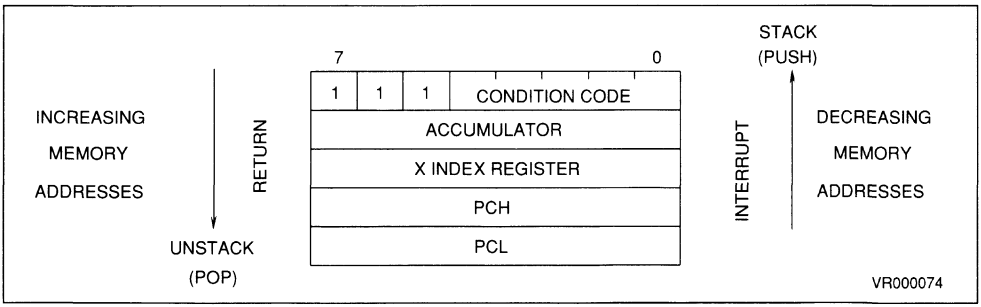
Interrupt mask (I). When the I bit is set to 1, all interrupts are disabled. Clearing this bit enables them. Interrupts requested while I is set are latched and can be processed when I is cleared (only one interrupt request per interrupt enable flag can be latched).

Negative (N). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is negative (i.e. the most significant bit is a logic 1).

Zero (Z). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

Carry/Borrow (C). When set, C indicates that a carry or borrow out of the ALU occurred during the last arithmetic operation. This bit is also affected during bit test, branch, shift and rotate instructions.

Figure 3. Stacking Order



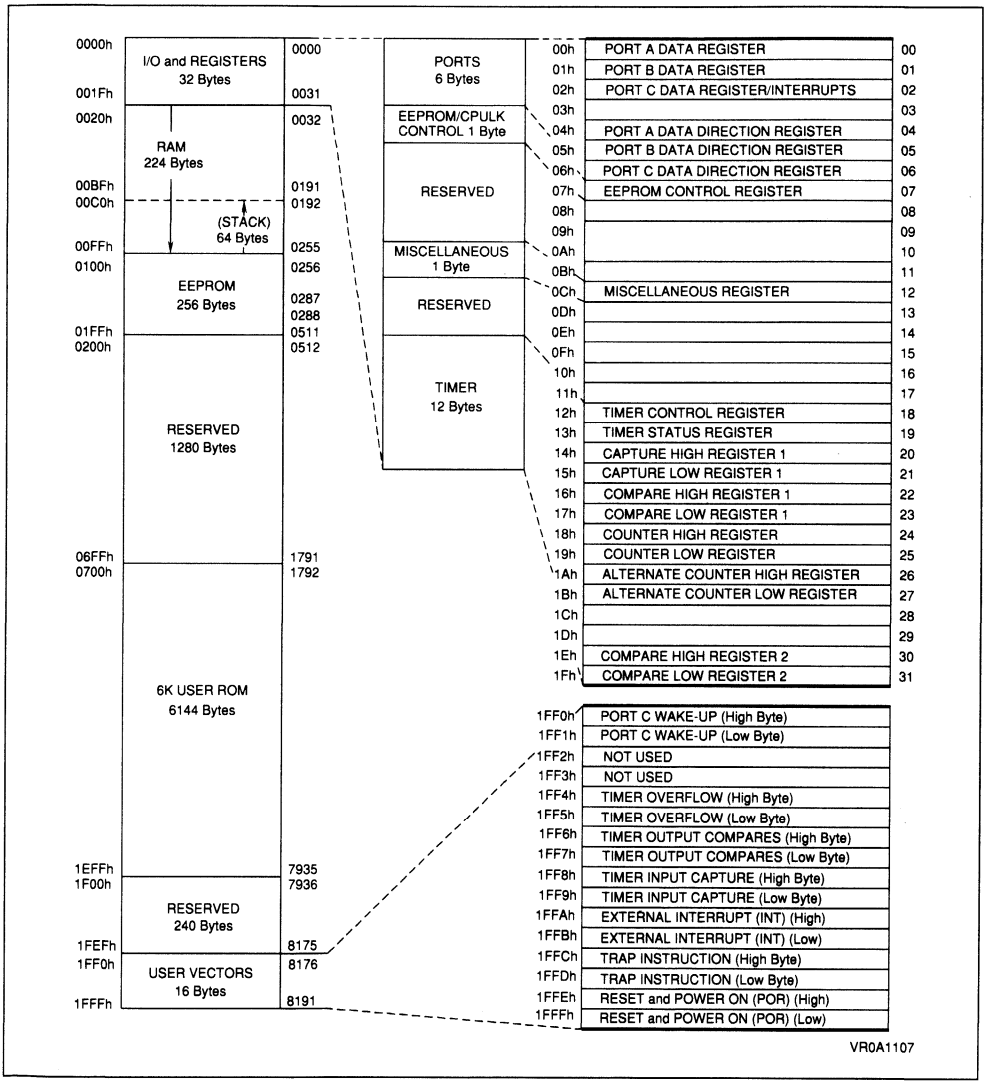
1.4 MEMORY MAP

As shown in Figure 4, the MCU is capable of addressing 8192 bytes of memory and I/O registers. In the ST7294, 6612 of these bytes are user accessible.

The locations consist of 32 bytes of I/O registers (only 20 are used), 224 bytes of RAM, 256 bytes of EEPROM and 6Kbytes of user ROM. The RAM space includes 64 bytes for the stack from 0FFh to 0C0h. Programs that only use a small part of the allocated stack locations for interrupts and/or subroutine stacking purpose can use the remaining bytes as standard RAM locations.

The highest address bytes contains the user defined reset and interrupt vectors.

Figure 4. Memory Map



1.5 WATCHDOG SYSTEM

The watchdog system consists in a divider-by-8 counter and a fixed divide-by-1024 prescaler. It is controlled through bit WDOG of the Miscellaneous Register. Two mask options are provided.

The watchdog enable mode mask option selects the state of the watchdog system after an external or a power-on reset. In the "programmable enable" option, a reset causes the watchdog to be disabled and the counter to be forced to zero. When the watchdog is configured with the "programmable enable" option, the watchdog system is enabled by setting the WDOG bit of the Miscellaneous Register (0Ch). Only an external or a power-on reset can clear WDOG and disable the watchdog system.

Whatever the option, when the watchdog counter is enabled, it is driven by the CPU clock through the divide-by-1024 prescaler (i.e. the counter clock period is 1024 CPU clock cycles). It is reset to zero by writing WDOG at 1. A system reset is generated if the counter reaches it maximum count (8). To avoid a system reset, the software must therefore reset the counter at least after a time tdog from the last clear or from the time the watchdog system has been enabled.

Care has to be taken when enabling the counter ("programmable enable" option only). The prescaler is actually in an unknown state at the time WDOG is set. The first rising edge can thus be sent to the watchdog counter after a time comprised between 0 and 1024 CPU clock cycles. In this mode, the first reset of the watchdog counter should therefore not occur later than 6x1024 CPU clock cycles after it has been enabled.

The system reset is generated by pulling down the RESET pin for at least one and a half CPU clock cycle. The state of the RESET pin is re-entered, thus causing an external reset to be issued.

The WATCHDOG DURING WAIT mask option allows to determine the watchdog function during the WAIT low power mode. In the "active during WAIT" option, the watchdog is kept active, thus able to reset the MCU if it remains in WAIT mode longer than the watchdog timeout period. In the "suspended during WAIT" option, it suspends operation during the WAIT mode and resets its counter. It will then resume operation when exiting the WAIT mode.

The HALT mode is inhibited when the watchdog system is enabled. However if a HALT instruction is executed while it is enabled, a watchdog reset is immediately generated.

1.6 MISCELLANEOUS REGISTER

Miscellaneous Register (000Ch)
Read/Write

Reset Value: 0001 000 (10h)

This register is a various 8-Bit register where only 4bits are used for interrupt, slow mode and Watchdog purposes.

7							0
—	INTP	INTN	—	—	—	SM	WDOG

b7, b4-b2 = Unused

b6 = **INTP**: *External Interrupt Positive* allows to select the INT line triggering mode in conjunction with INTN. It can only be modified when the I bit of the CCR is set.

b5 = **ININ** :*External Interrupt Negative* allows to select the INT line triggering mode in conjunction with INTP. It can only be modified when the I bit of the CCR is set.

b1 = **SM**: *Slow Mode.* Setting this bit to "1" enables Slow Mode, thus reducing power consumption. In this mode, an extra divider by 16 is added in the clock circuitry.

b0 = **WDOG**: *Watchdog System.* Whatever the WATCHDOG ENABLE MODE mask option, the watchdog counter is reset when WDOG is written at 1. When the MCU is configured with the "programmable enable" option, the WDOG bit is low after a reset. It must be set to enable the watchdog system. Only a reset can clear WDOG.

1.7 CLOCK SYSTEM

1.7.1 General Description

The MCU accepts either a Crystal/Ceramic resonator or an external clock to provide the internal oscillator. The internal clock (fop) is derived by a divide-by-2 from the external oscillator frequency (fosc).

The slow mode function allows under software control to further slow down the internal clock, thus reducing power consumption. This feature is particular useful in WAIT mode.

The slow mode is entered by setting the SM bit in the Miscellaneous Register (0Ch). This mode affects all functions, including timer and EEPROM. The slow mode is exited by clearing SM or by entering the STOP mode.

Crystal . The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for fosc. The circuit shown on Figure 5 is recommended when using a crystal. The table lists the recommended capacitance and feedback resistance values.

Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and startup stabilization time.

Ceramic Resonator. A ceramic resonator may be used in place of the crystal in low cost applications. The circuit on Figure 5 is recommended when using a ceramic resonator. The table lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

External Clock. An external clock should be applied to the OSCin input with the OSCout pin not connected, as shown on Figure 6. The t_{OXOV} and t_{ILCH} specifications do not apply when using an external clock input. The equivalent specification of the external clock source should be used instead of t_{OXOV} or t_{ILCH}.

Figure 5. Crystal/Ceramic Resonator

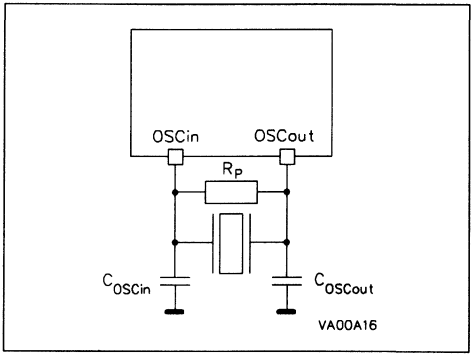
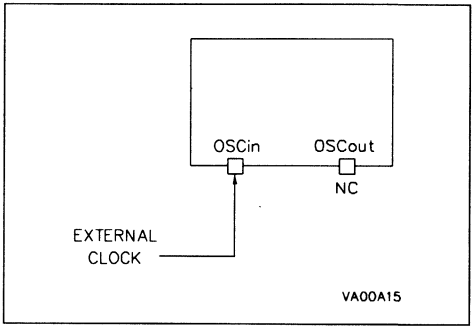
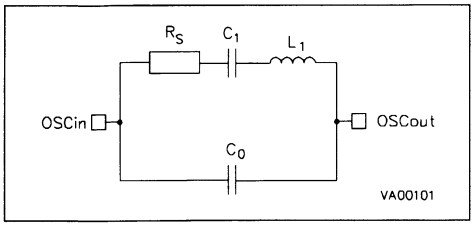


Figure 6. External Clock Source Connections



CLOCK SYSTEM (Continued)

Figure 7. Equivalent Crystal Circuit



Recommended Settings for Crystal

	2MHz	4MHz	Unit
R_{SMAX}	400	75	Ω
C_0	5	7	pF
C_1	0.008	0.012	pF
C_{OSCin}	15-40	15-30	pF
C_{OSCout}	15-30	15-25	pF
R_P	10	10	MΩ
Q	30	40	10^3

Recommended Settings for Ceramic Resonator

	2-4MHz	Unit
R_{SMAX}	10	Ω
C_0	40	pF
C_1	4.3	pF
C_{OSCin}	30	pF
C_{OSCout}	30	pF
R_P	1-10	MΩ
Q	1250	

1.8 RESETS AND INTERRUPTS

Resets are used to provide an orderly software startup procedure or to quit low power modes.

Two reset modes are provided: a power-on reset and an external reset at pin RESET. The watchdog reset is considered as an external one though the watchdog system generates a MCU reset by pulling down the RESET pin.

A summary of the effects of both reset modes on the different sections of the MCU is given in the following Table. For further information, please refer to the part describing the particular section.

1.8.1 External Reset

The external reset is an active low input signal applied to the RESET pin of the MCU.

As shown in Figure 8, the RESET signal must stay low for a minimum of one and a half CPU clock cycles. A reset causes the reset vector to be fetched at addresses 01FFEh and 01FFFh in order to be loaded into the PC.

The external reset is used by the watchdog system to reset the MCU. When active, the power-on reset circuitry pulls down the RESET pin. In both cases, the RESET pin can be used as an output to reset other devices. However, the pull down circuitry features a current limitation to allow the connection of any input signal, including from an RC type circuit.

An internal Schmitt trigger at pin RESET improves noise immunity.

1.8.2 Power-on Reset (POR)

The power-on reset (POR) is generated upon detection of a positive transition on V_{DD} (refer to Figure 8). It causes the reset vector to be fetched at addresses 01FFEh and 01FFFh in order to be loaded into the PC.

An internal circuitry provides a 4096 CPU clock cycle delay from the time the oscillator becomes active. At the end of the power-on reset, the MCU can be maintained in the reset condition by the external reset. The RESET pin can therefore be used to ensure V_{DD} has risen to a point where the MCU can properly operate before running the MCU program.

RESET AND INTERRUPTS (Continued)

During the POR, the RESET pin is pulled low, thus permitting the MCU to reset other devices.

The power-on reset is strictly used for power up conditions and should not be used to detect any drop in the power supply voltage. There is no provision for a power-down reset.

1.8.3 Interrupts

The ST7294 may be interrupted by one of four different methods: the three maskable hardware interrupts (INT, PORT C, or TIMER) and the non-maskable software interrupt (TRAP). The Interrupt processing flowchart is shown in Figure 9. The maskable interrupts must be enabled in order to be serviced. However, disabled interrupts can be latched and processed when they are enabled. When an interrupt has to be serviced, the PC, X, A and CC registers are saved into the stack and the interrupt mask (I bit of the Condition Code Register) is set to prevent additional interrupts. The Y register is not automatically saved. The stack order is shown on Figure 3.

The PC is then loaded with the interrupt vector of the interrupt to service and the interrupt service routine runs (refer to Table 3 for vector addresses). It should finish by the IRET instruction which causes the contents of the registers to be recovered from the stack and normal processing to resume. Note that the I bit is then cleared if and only if the corresponding bit stored in the stack is zero.

Though many interrupts can be simultaneously pending, a priority order is defined (see Table 4). The RESET pin has the highest priority. Then, if the I bit is low, the decreasing priority order is TRAP, INT, timer input capture, timer output compare, timer overflow and PORT C. If the I bit is set, TRAP is the only enabled interrupt.

Interrupts allow the processor to leave low power modes. Refer to LOW POWER MODES for further information.

Software Interrupt. The software interrupt is the TRAP executable instruction. The interrupt is recognized when the TRAP instruction is executed, regardless to the I bit state. When the interrupt is recognized, it is serviced according to the flowchart on Figure 9.

External Interrupt. The external interrupt is generated through the INT pin. The interrupt is enabled if the I bit of the CCR is cleared.

Table 2. List of sections affected by RESET, WAIT and HALT

Section	RESET	POR	WAIT	HALT
Timer Prescaler reset to zero	X	X	-	-
Timer Counter set to FFFCh	X	X	-	-
All Timer enable bit set to 0 (disable)	X	X	-	-
Data Direction Regfisters set to 0 (as Inputs)	X	X	-	-
Set Stack Pointer to 00FFh	X	X	-	-
Force Internal Address Bus to restart vector 1FFEh, 1FFFh	X	X	-	-
Set Interrupt Mask Bit (I-Bit, CCR) to 1 (Interrupt Disable)	X	X	-	-
Set Interrupt Mask Bit (I-Bit, CCR) to 0 (Interrupt Enable)	-	-	X	X
Reset HALT Latch	X	X	-	-
Reset INT Latch	X	X	-	-
Reset WAIT Latch	X	X	-	-
Disable fop Clock (for 4096 cycles)	-	X	-	X
Set CPU Clock to 0	-	X	X	X
Set Timer Clock to 0	-	X	-	X
SM-Bit cleared	X	X	-	X
Watchdog counter reset	X	X	-	X
Watchdog WDOG-BIT reset	X	X	-	X
EEPROMs control bits reset	X	X	-	-

RESET AND INTERRUPTS (Continued)

The INTN and INTP bits of the Miscellaneous Register (0Ch) allow selection of the interrupt triggering mode among the 4 available ones. Refer to Table 3 for the triggering mode coding.

In order to avoid conflicts and spurious interrupts, the external interrupt options can only be changed when the I bit is set. Any attempt to change the options while I is reset fails. When the options are changed any pending interrupt is lost.

When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution. It is then processed according to the flowchart on Figure 9.

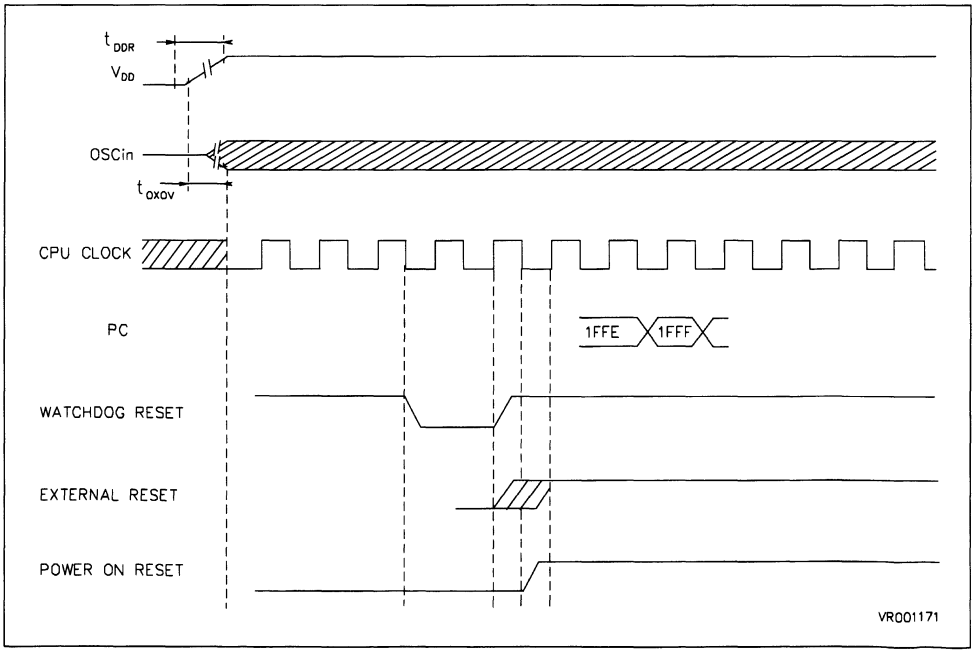
If the interrupt is disabled (I high), the triggering edge of the INT line is internally latched and the interrupt remains pending to be processed as soon as the interrupt is enabled (the low level sensitive interrupt is not latched and can therefore not remain pending). This internal latch is cleared in the first part of the service routine. Therefore, one, and one only, external interrupt can be latched and serviced as soon as enabled.

Figure 10 shows the mode timing diagram for the interrupt line. Two methods are described. The first method shows single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an IRET instruction occurs).

The second configuration shows several interrupt lines "wire-ORed" to form the interrupts at the processor. Thus, if after servicing one interrupt the interrupt line remains low, then the next interrupt is recognized.

PORTC Interrupt. The PORTC Interrupt can be generated on the falling edge of one pin PC0-PC5 if it is defined as an interrrupt source. When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution. It is then processed according to the flowchart on Figure 9.

Figure 8. Reset Timing Diagram

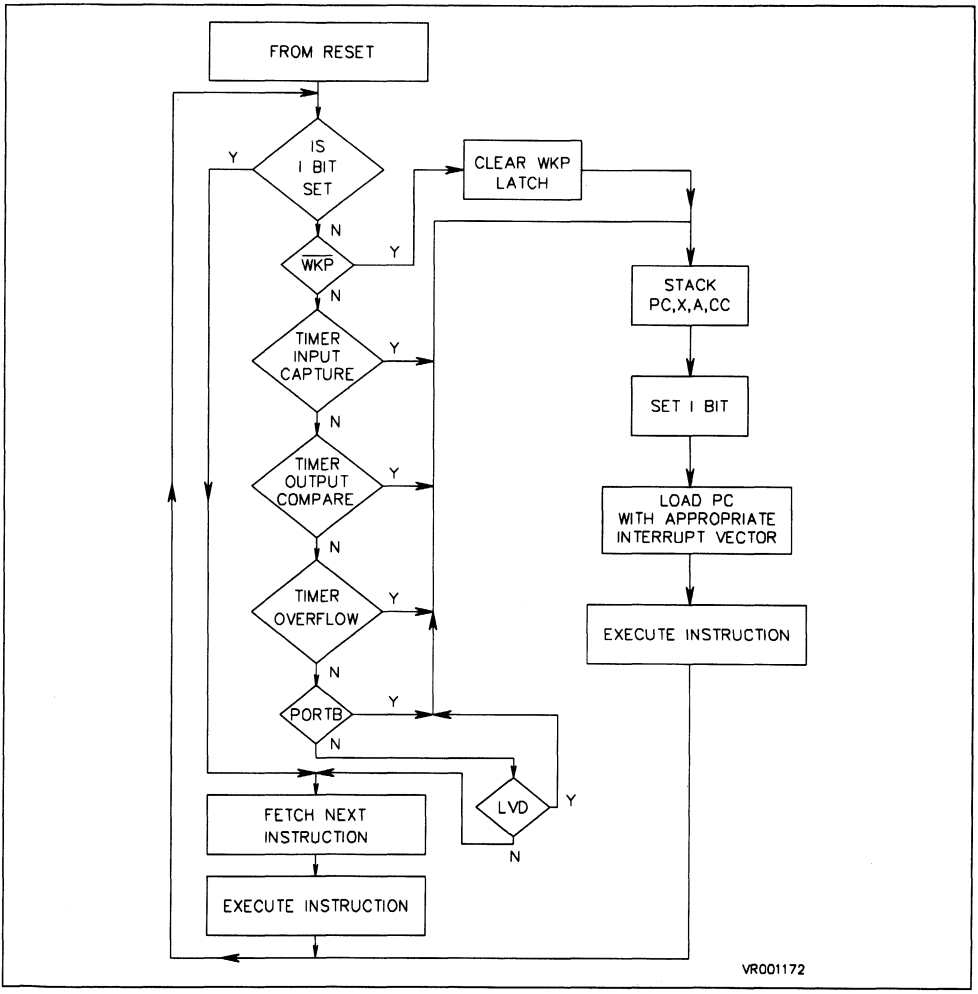


RESET AND INTERRUPTS (Continued)

Table 3. External Interrupt Options

INTP	INTN	External Interrupt Options
0	0	Negative edge and Low level sensitive
0	1	Negative edge only
1	0	Positive edge only
1	1	Positive and negative edge sensitive

Figure 9. Interrupt Processing Flow-Chart



RESET AND INTERRUPTS (Continued)

If the interrupt is disabled (I high), the triggering edge of the wake-up interrupt sources logical-OR is internally latched and the interrupt remains pending to be processed as soon as the interrupt is enabled. This internal latch is cleared in the first part of the service routine. Therefore, one and one only external interrupt can be latched and serviced as soon as possible.

Timer Interrupt. Four different timer interrupt flags are able to cause a timer interrupt when they are active if both the I bit of the CCR is reset and if the corresponding enable bit is set. If either of these conditions is false, the interrupt is latched and thus remains pending.

The interrupt flags are located in the Timer Status Register (0013h). The Enable bit are in the Timer Control Register (0012h).

When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution. it is then serviced according to the flowchart on Figure 9. Software in the timer service routine must determine the priority and cause of the timer interrupt by examining the interrupt flags and the status bits located in the TSR.

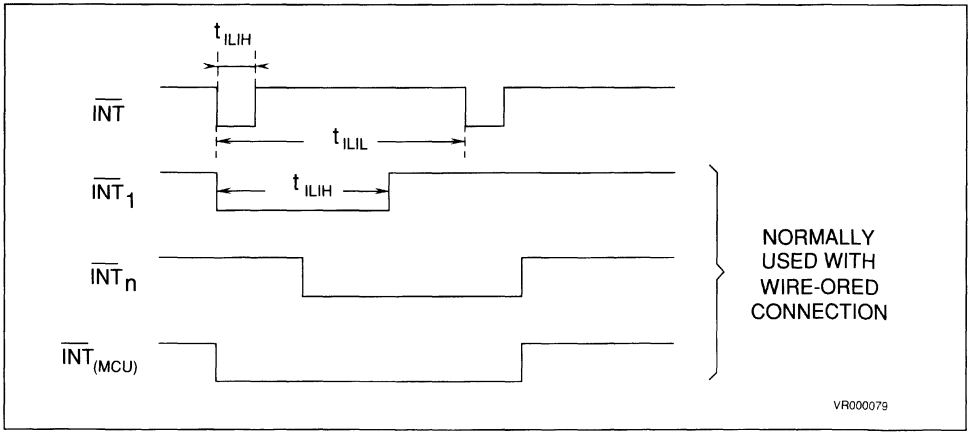
The general sequence for clearing an interrupt is an access to the status register while the flag is set followed by a read or write of an associated register. Note that the clearing sequence resets the internal latch. A pending interrupt (i.e. waiting for being enabled) will therefore be lost if the clear sequence is executed.

Refer to 16 BIT TIMER for further information.

Table 4. Interrupt and Reset priorities

Vector Address	Interrupt Source	Masked by	Priority
1FFEh,1FFFh	RESET and POWER-ON (POR)	none	Highest
1FFCh,1FFDh	SOFTWARE Interrupt (TRAP)	none	
1FFAh,1FFBh	EXTERNAL Interrupt (INT)	I-Bit	
1FF8h,1FF9h	TIMER INPUT Capture	I-Bit	
1FF6h,1FF7h	TIMER OUTPUT Compares (1 and 2)	I-Bit	
1FF4h,1FF5h	TIMER OVERFLOW	I-Bit	
1FF2h,1FF3h	Reserved	I-Bit	
1FF0h,1FF1h	PORTC Wake-up	I-Bit	Lowest

Figure 10. Timing Diagram for Interrupt Line



1.9 LOW POWER MODES

Table 2 gives a list of the different sections affected by the low power modes. For detailed information on a particular devices, please refer to the corresponding parts.

HALT Mode. The HALT mode is the MCU lowest power consumption mode. The HALT mode is entered by executing the HALT instruction. The internal oscillator is then turned off, causing all internal processing to be stopped, including the operation of the on-chip peripherals. The HALT mode cannot be used when the watchdog is enabled, if the HALT instruction is executed while the watchdog system is enabled, a watchdog reset is generated thus resetting the entire MCU.

When entering the HALT mode, the I bit in the Condition Code Register and the SM bit in the Miscellaneous Register are cleared. Thus, the external interrupts are allowed and the MCU is placed at its nominal speed (see CLOCK SYSTEM). All other registers and memory remain unaltered and all I/O lines remain unchanged.

The MCU can exit the HALT mode upon reception of either an external interrupt or PORTC or a power-on or external reset. The oscillator is then turned on and a stabilization time is provided before releasing CPU operation. The stabilization time is 4096 CPU clock cycles.

After the start up delay, the CPU continues operation by servicing the interrupt which wakes it up or by fetching the reset vector if a reset wakes it up.

WAIT Mode. This mode is a low power consumption mode, but the power consumption is higher than in the HALT mode. The consumption can be further reduced by entering the slow mode.

The WFI instruction places the MCU in the WAIT mode.

In the WAIT mode, the internal clock remains active but all CPU processing is stopped; however, the programmable timer remains in his previous state. The watchdog can either be active or not according to the WATCHDOG DURING WAIT mask option.

During the WAIT mode, the I bit in the condition code register is cleared to enable all interrupts.

All other registers and memory remain unaltered and all parallel I/O lines remain unchanged.

An interrupt or a reset causes the MCU to exit the WAIT mode. An interrupt while the MCU is in the WAIT mode causes the corresponding interrupt vector to be fetched, the interrupt routine to be executed and normal processing to resume. A reset causes the program counter to fetch the reset vector and processing starts as for a normal reset.

DATA RETENTION Mode. The contents of RAM and CPU registers are retained at supply voltage as low as 2.0 volts. This is referred to as the data retention mode, where the data is held, but the device is not guaranteed to operate.

LOW POWER MODES (Continued)

Figure 11. HALT Function Flow Chart

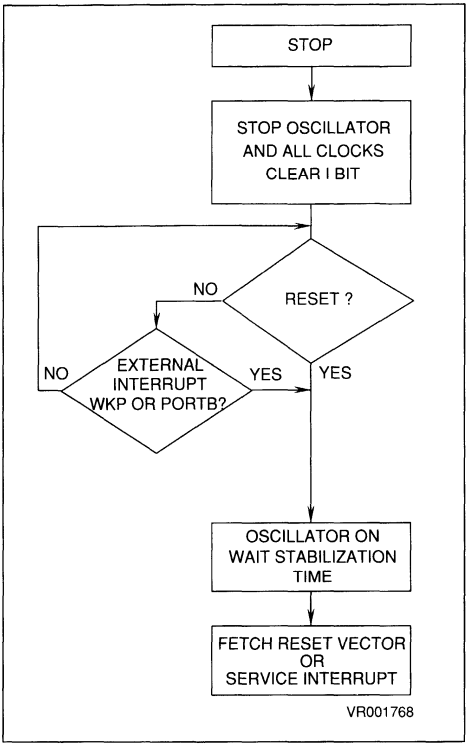
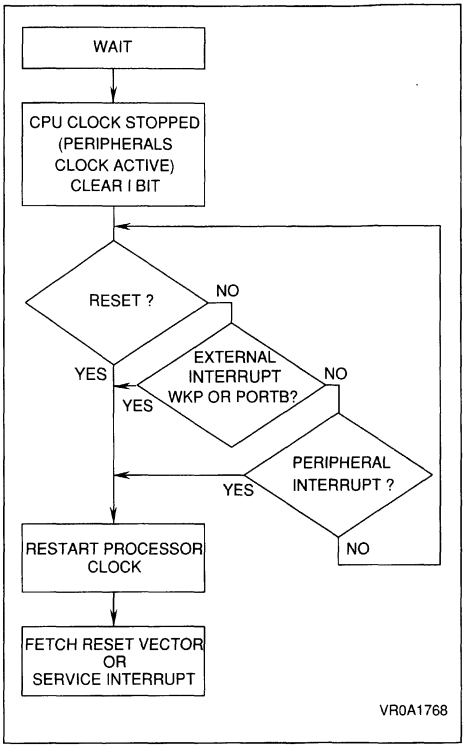


Figure 12. WAIT Flow Chart



2 FUNCTIONS DESCRIPTION

2.1 EEPROM

An internal charge pump avoids the need of external high voltage supply for the erase and programming functions.

8 data registers allow simultaneous write or erase of 1 to 8 bytes in the EEPROM array.

2.1.1 Functional Description

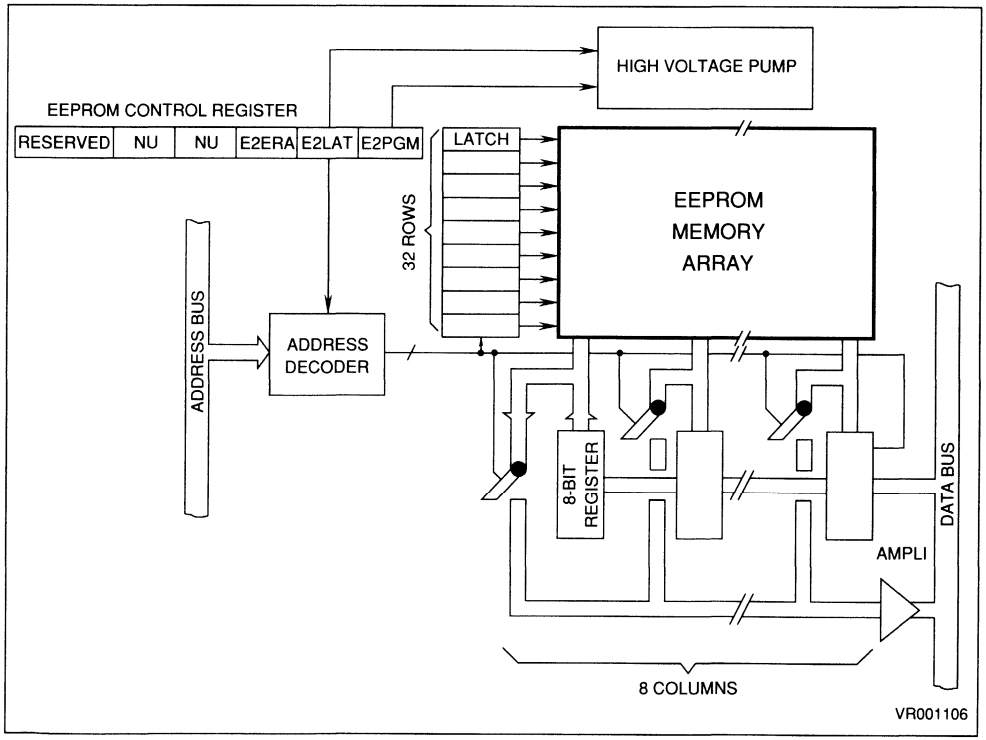
As shown on Figure 22, the EEPROM is a 8 columns by 32 rows array. The row is selected by the A7, A6, A5, A4, A3 bits. Each column is associated to an 8-bit data register.

Read Operation (E2LAT=0).
The EEPROM can be read as a normal ROM when the E2LAT bit of the Control Register is low. When E2LAT is low, the E2PGM and E2ERA bits are forced low.

Write/Erase Operation. (E2LAT=1)
When E2LAT is set to "1", a write to an EEPROM location latches the data in the 8-bit register corresponding to the decoded column and marks the decoded row.
As there are 8 columns in each row, up to 8 locations (having the same A7, A6, A5, A4, A3 address bits) can be simultaneously written or erased.

To **erase** bytes, set the E2LAT and E2ERA bits, then write to the EEPROM addresses to be erased (data value is not significant) and at least set the E2PGM bit to turn the charge pump on.
To **write** bytes, set the E2LAT bit, then write the data in the appropriate EEPROM addresses, and at least set the E2PGM bit to turn the charge pump on.

Figure 13. EEPROM Block Diagram



EEPROM (Continued)

Note 1. It is mandatory to erase bytes before writting them.

Note 2. E2LAT must be kept high during a time tprog and then be cleared .

Note 3. When E2LAT is high, access to the EEPROM array is impossible.

Note 4. It is impossible to perform successives write or erase without clearing E2LAT.

Warning. User programs must not run from the EEPROM (only data space).

EEPROM CONTROL REGISTER (07h)

Read/Write
Reset Value: 0000 0000 (00h)

7							0
Res	Res	Res	—	—	E3ERA	E2LAT	E2PGM

This register contains the bits required to read, erase and program the EEPROM. They are defined as follow:

Bit 7, 6, 5 = Reserved

Bit 4,3 = Unused

Bit 2 = **E2ERA** *EEPROM Erase*
E2ERA must be set to "1" for an erase operation. It must be set after or at the same time as E2LAT. It cannot be changed once 1 EEPROM address is selected. It is held low when E2LAT is low. It is therefore automatically reset when E2LAT is reset.

Bit 1 = **E2LAT** *EEPROM Latch Enable*
When E2LAT is reset to "0", data can be read from the EEPROM. When it is set to "1" and E2PGM reset to "0", a write into the EEPROM array causes the data to be latched, according to the address into one of 8 data registers. An additional bit is latched to select the row. The selected columns and row determine the locations involved in the next erase or programming operation. E2LAT must be cleared after each programming or erase operation. E2ERA and E2PGM are forced low when E2LAT is low.

Bit 0 = **E2PGM** *EEPROM Program Mode*
This bit allows to switch on or off the internal charge pump. When set to "1", the charge pump generator is on: the high voltage is applied to the EEPROM array. When low, the charge pump generator is off. E2PGM can only be reset by resetting E2LAT.

2.2 I/O PORTS

2.2.1 Functional Description

Ports A, B are 8-bit I/O ports, port C is a 6-bit I/O port. Each of their pins can be individually configured under software control as either input or output.

Each bit of any DDR corresponds to an I/O pin of the associated port. A bit must be set to configure its associated pin as output and must be cleared to configure its associated pin as input. The Data Direction Registers can be written or read.

The typical I/O circuit is shown on Figure 14. Any write to an I/O port updates the port output register even if it is configured as input. Any read of an I/O port returns either the data latched in the port output register (output configured pins) or the value at the I/O pin (input configured pins) (see Table 6).

At power-on or external reset, all DDR's are cleared, which configures all port A, B and C pins as inputs, but the port output registers are not initialized. Thus, the I/O port should be written to before setting the DDR bit to avoid undefined levels.

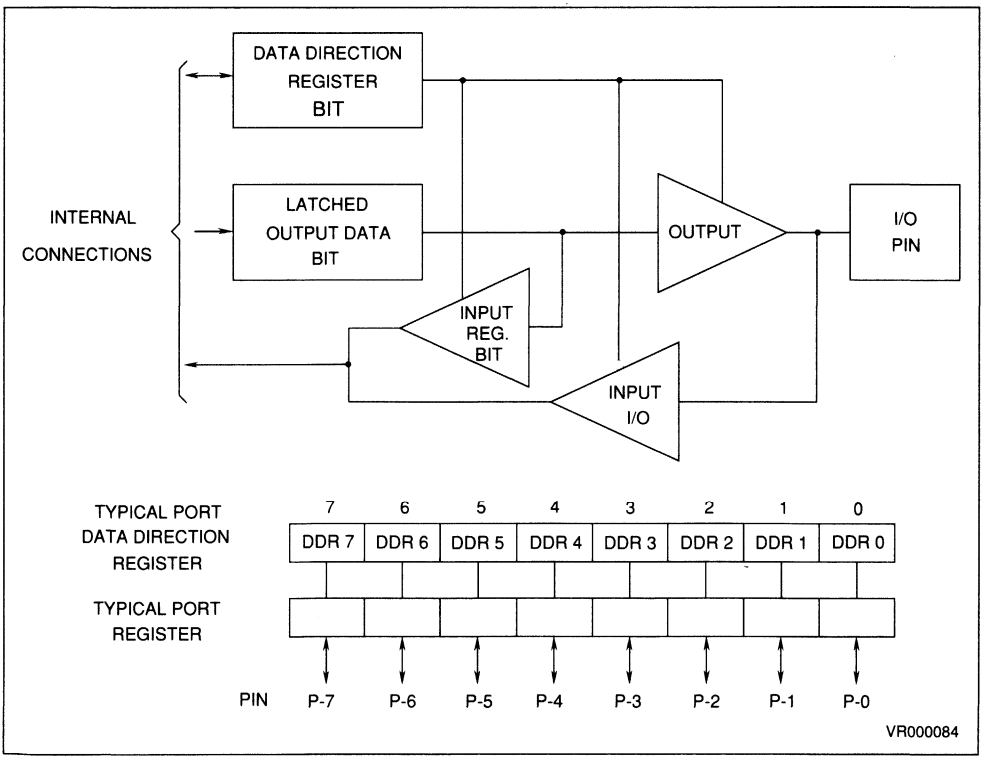
According to mask option, each Port A bit can be defined as an Input/Output line or as an Input/Output drain line. When programmed as input, each port line may be tied to V_{DD} through an internal pull-up resistor (by option).

According to mask option, each PORT B bit can be tied to V_{DD} through an internal pull-up resistor if defined as input.

According to mask option, each PORT C bit can be configured as wake-up interrupt input with an internal pull-up resistor. To enter this mode, the corresponding bit in DDR must be set to 1 and the corresponding bit in DR must be set to 0.
This mode can only be reached for PC0 and PC1 if they have not been configured as ICAP or OCMP1 respectively.

All unused I/O lines should be tied to an appropriate logic level (either V_{DD} or V_{SS}).

Figure 14. I/O Pin Typical Circuit



I/O PORTS (Continued)

Table 6. I/O Pin Functions

R/$\overline{W}$*	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

* R/$\overline{W}$ is an internal signal.

DATA REGISTERS

Port A: 00h
Port B: 01h
Port C: 03h

Read/Write

Reset Value: Undefined

7							0
MSB							LSB

DATA DIRECTION REGISTERS

Port A: 04h
Port B: 05h
Port C: 06h

Read/Write

Reset Value: 00h (as inputs)

7							0
MSB							LSB

2.3 16 BIT TIMER

The 16-bit programmable timer consists of a 16-bit free running counter driven by a mask option configurable prescaler and control logic for one input capture and two output compare registers. It can be used for many purposes including pulse length measurement of one input signal and generation of one output waveform.

Pulse lengths and waveform periods can vary from several microseconds to many seconds because of the mask option configurable prescaler. When used with a 4MHz CPU clock, the timer has a resolution of either 0.5, 1 or 2ms according to the selected TIMER CLOCK mask option.

Because the timer has a 16-bit architecture, each of its specific function block is represented by two registers. These registers contain the high order byte and low order byte of that function. However an access to the high order byte inhibits that specific timer capability until the low order byte is also accessed.

Note that correct software procedures should set the I bit of the Condition Code Register before accessing the high order byte to prevent an interrupt from occurring between the accesses to the high and low order bytes of any register.

The timer block diagram is shown on Figure 14:

Table 7. Timer Clock Mask Options

Option	Timer Prescaler directed by ratio (1)
Slow	8
Standard	4
Fast	2

Note 1 : The timer clock is obtained by dividing the internal clock by the prescaler ratio.

2.3.1 Functional Description

Counter. The key element of the programmable timer is a 16-bit free running counter or counter register. It is preceded by a prescaler which divides the internal clock by two, four or eight according to the selected TIMER CLOCK mask option (see Table 7).

Software can read the counter at any time without affecting its value. It can be read from two locations, the Counter Register (0018h, 0019h) and Alternate Counter Register (001Ah, 001Bh). The only difference between these two read-only registers is the way the overflow flag TOF is handled during a read sequence.

A read sequence containing only a read of the least significant byte of the free running counter (from either the Counter Register or the Alternate Counter Register) will receive the LSB of the count value at the time of the read. A read of the most significant byte (from either the Counter Register or the Alternate Counter Register) simultaneously returns the MSB of the count value and causes the LSB to be transferred into a buffer.

The buffered value remains unchanged until the 16-bit read sequence is completed, even if the user reads the MSB several times. The read sequence is completed by reading the free running counter LSB, which actually returns the buffered value.

As shown on Figures 16, 17 and 18, the free running counter is configured to FFFCh during reset. During a power-on reset (POR), the counter is also configured to FFFCh and begins running after the oscillator startup delay.

When the counter rolls over from FFFFh to 0000h, the Timer Overflow flag (TOF) of the Timer Status Register (TSR) is set. A timer interrupt is then generated if the TOIE enable bit of the Timer Control Register (TCR) is set, provided the I bit of the CCR is cleared. If one of these conditions is false, the interrupt remains pending to be issued as soon as they are both true. The interrupt request is cleared by reading TSR while TOF is set followed by an access (read or write) to the LSB of the Counter Register.

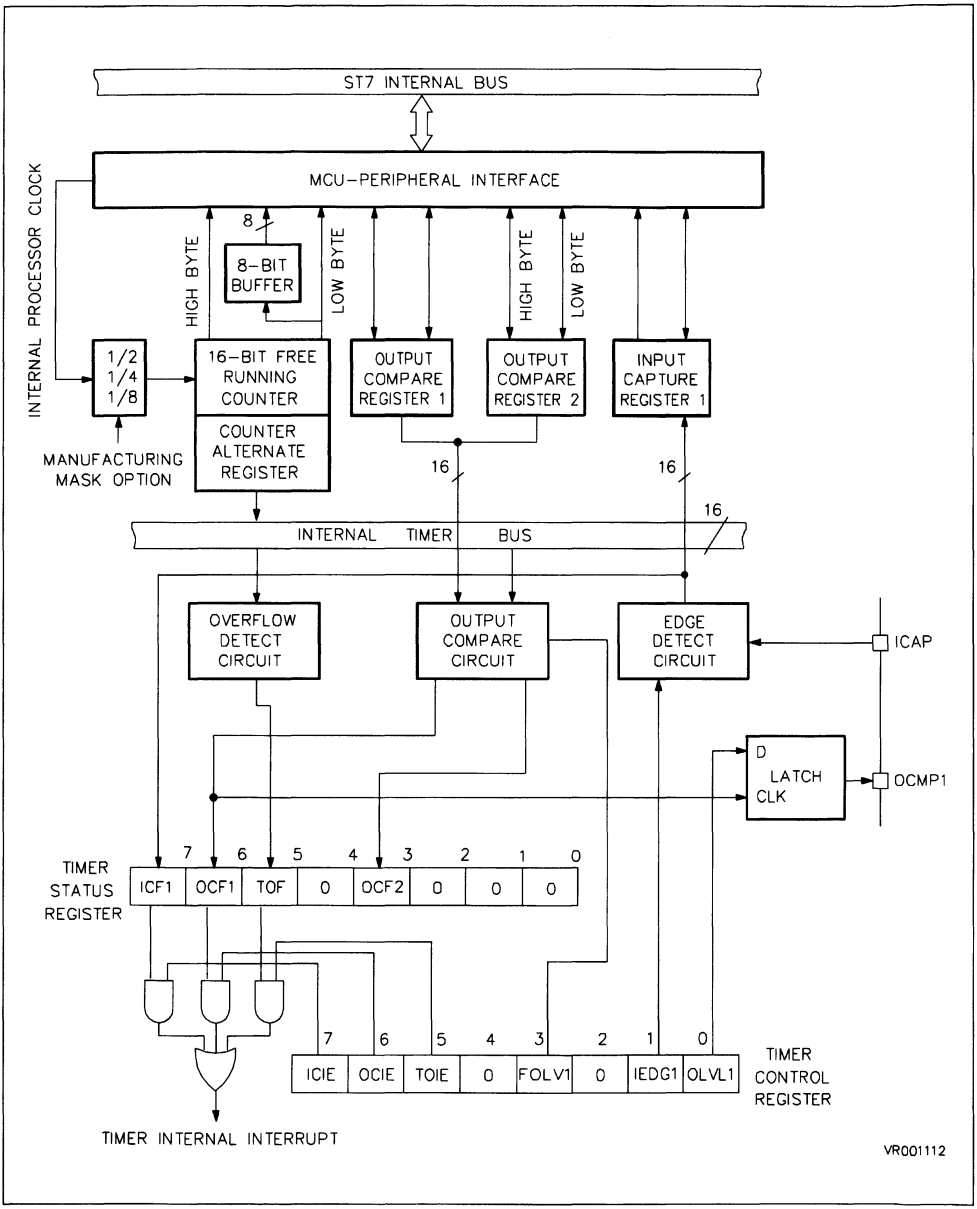
The TOF flag is not affected by accesses to the Alternate Counter Register. This feature allows simultaneous use of the overflow function and reads of the free running counter at random times (for example, to measure on elapsed time) without risking to clear the TOF flag erroneously. Accesses to the timer without the intention of servicing the TOF flag should therefore be performed to the Alternate Counter Register while only the TOF service routine accesses the Counter Register.

The free running counter can be reset under software control. This is performed by writing to the LSB of either the Counter Register or the Alternate Counter Register. The counter and the prescaler are then configured to their reset conditions. This reset also completes any 16-bit access sequence. All flags and enable bits are unchanged.

The value in the counter registers repeats every either 131072, 262144, or 524288 internal processor clock cycles according to the TIMER CLOCK option. As shown on Figures 16, 17 and 18, the counter increment is triggered by a falling edge of the CPU clock.

16 BIT TIMER (Continued)

Figure 15. Timer Block Diagram



16 BIT TIMER (Continued)

Figure 16. Timer Timing Diagram, Fast Mask Option

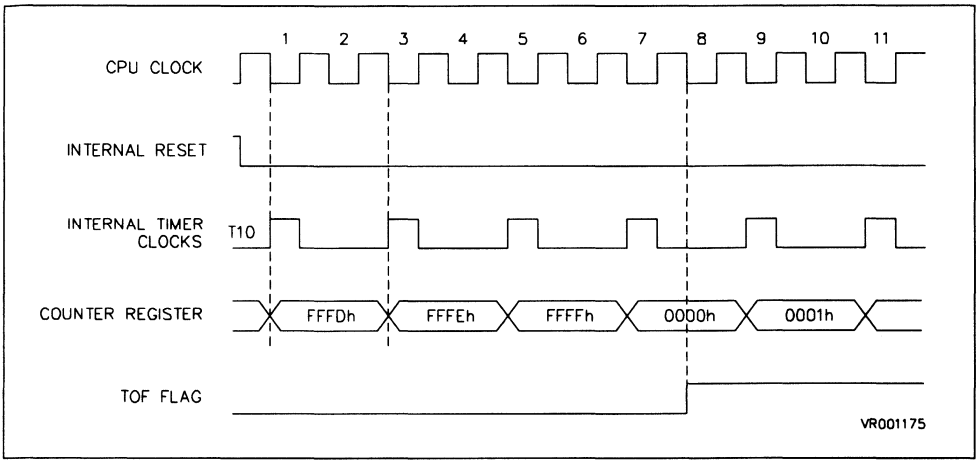
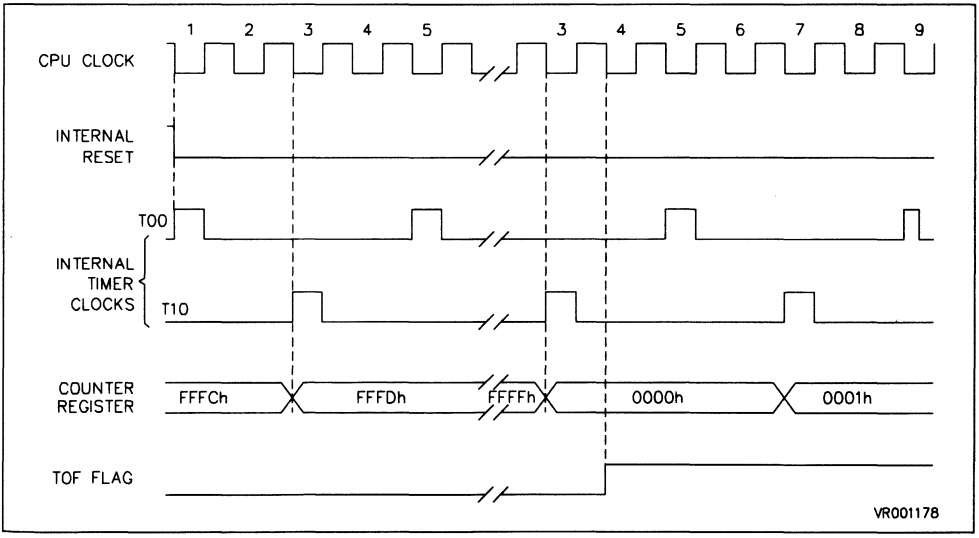
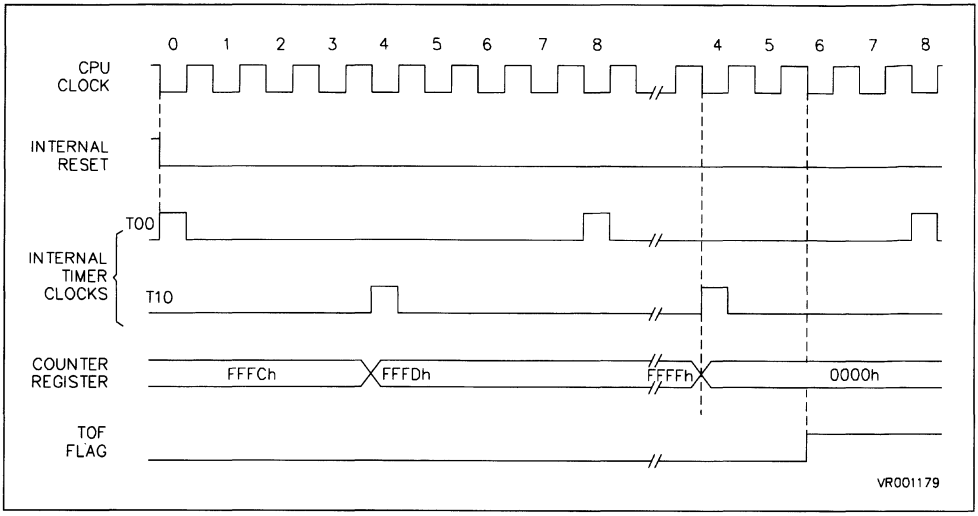


Figure 17. Timer Timing Diagram, Standard Mask Option



16 BIT TIMER (Continued)

Figure 18. Timer Timing Diagram, Slow Mask Option



The timer is not affected by the WAIT mode. In the HALT mode, the counter stops counting until the mode is exited. Counting then resumes from previous count (MCU awaken by an interrupt) or from reset count (MCU awaken by a reset).

Input Capture. The ST7294 features one input capture register and one input capture interrupt enable bit.

Input Capture Register (ICR1) is a 16-bit register made up of two 8-bit registers: the most significant byte register (ICHR1), located at 014h, and the least significant byte register (ICLR1) located at 015h.

ICR1 is a read-only register used to latch the value of the free running counter after a defined transition is sensed by the input capture edge detector at pin ICAP. This transition is software programmable through the IEDG1 bit of the Timer Control Register (TCR). When IEDG1 is set, a rising edge triggers the capture; when IEDG1 is low, the capture is triggered by a falling edge.

When an input capture occurs, the flag ICF1 in Timer Status Register (TSR) is set. An interrupt is requested if the interrupt enable bit ICIE of TCR is set, provided the I bit of the CCR is cleared. Otherwise, the interrupt remains pending until both conditions becomes true. It is cleared by reading the TSR followed by an access (read or write) to the LSB of ICR1.

The result stored in ICR1 is one more than the value of the free running counter on the rising edge of the internal processor clock preceding the active transition at pin ICAP (see Figure 19). This delay is required for internal synchronization. Therefore, the timing resolution of the input capture system is one count of the free running counter, i.e. 2, 4 or 8 internal clock cycles according to the selected TIMER CLOCK mask option.

The free running counter is transferred to ICR1 on each proper signal transition regardless of whether the Input Capture Flag ICF1 is set or cleared. The ICR1 always contains the free running counter value which corresponds to the most recent input capture.

After a read of the MSB of ICR1 (ICHR1), counter transfer of input capture is inhibited until the LSB of ICR1 (ICLR1) is also read. This characteristic forces the minimum pulse period attainable to be determined by the time to service the interrupt and to execute the interrupt routine.

A read of ICLR1 does not inhibit the counter transfer. Again, minimum pulse periods are the ones which allow software to read the least significant byte and perform needed operations. There is no conflict between the read of ICR1 and the running counter transfer since they occur on opposite edges of the internal processor clock (see Figure 19).

16 BIT TIMER (Continued)

The ICR1 is undetermined at power-on and is not affected by an external reset. Hardware circuitry has to provide protection from generating a wrong input capture when changing the edge sensitivity option of ICAP pin through the IEDG1 bit.

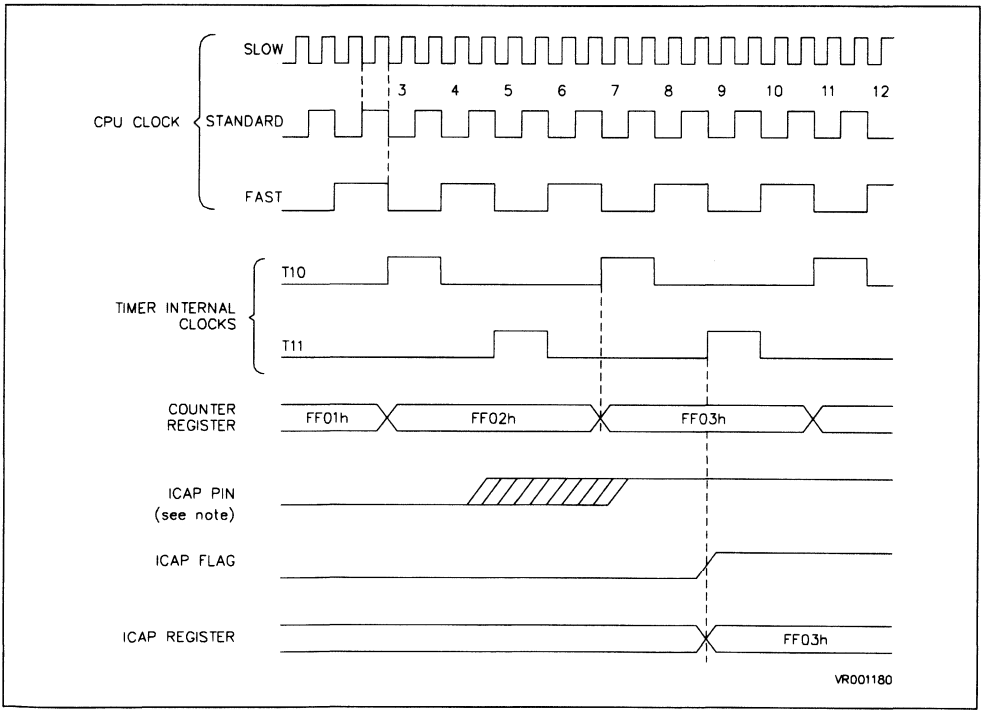
During the HALT mode, if at least one valid input capture edge occurs at the ICAP pin, the input capture detect circuitry is armed. This action does not set any timer flags nor "wake-up" the MCU. If the MCU is awaken by an interrupt, there is an active input capture flag and data from the first valid edge that occurred during the HALT mode. If the HALT mode is exited by a reset, the input capture detect circuitry is reset and thus, any active edge that happened during the HALT mode is lost.

Output Compare. There are two output compare registers: Output Compare Register 1 and 2 (OCR1 and OCR2). They can be used for several purposes such as controlling an output waveform or indicating when a period of time has elapsed. OCMP1 pin is associated with output compare 1; no pin is associated with output compare 2.

The Output Compare Registers are unique because all bits are readable and writable and are not affected by the timer hardware and reset. If a compare function is not used, the two bytes of the corresponding Output Compare Registers can be used as storage locations. Note that the same output compare interrupt enable bit is used for both output compares.

Output Compare Register 1. The Output Compare Register 1 (OCR1) is a 16-bit register, which is made up of two 8-bit registers: The most significant byte register (OCHR1) at address 0016h and the least significant byte register (OCLR1) at address 0017h.

Figure 19. Input Capture Timing Diagram



Note . The diagram represents the case of a rising edge sensitivity (IEDG1=1). The capture is performed at the next rising edge of T11, if the action edge of ICAP happened before the previous T10 falling edge.

16 BIT TIMER (Continued)

The content of OCR1 is compared with the content of the free running counter once during every timer clock cycles, i.e. once every 8, 4 or 2 internal processor clock periods according to the TIMER CLOCK mask option. If match is found, the Output Compare Flag OCF1 of the TSR is set and the Output Level bit (OLVL1) of the TCR is clocked to the OCMP1 pin (see output compare timing diagram on Figures 19, 20, 21).

OLVL1 is copied to the corresponding output level latch and hence, to the OCMP1 pin regardless of whether the Output Compare Flag (OCF1) is set or not. The value in the OCR1 and the OLVL1 bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout.

An interrupt accompanies a successful output compare if the corresponding interrupt enable bit OCIE of the TCR is set, provided the I-bit of the CCR is cleared. Otherwise, the interrupt remains pending until both conditions are true. It is cleared by a read of TSR followed by an access to the LSB of the OCR1.

After a processor write cycle to the OCHR1 register, the output compare function is inhibited until the OCLR1 is also written. Thus, the user must write both bytes if the MSB is written first. A write made to only the LSB will not inhibit the compare function. The minimum time between two successive edges on the OCMP1 pin is a function of the software program and the selected TIMER CLOCK option mask.

The OCMP1 output latch is forced low during reset and stays low until valid compares change it to a high level. Because the OCF1 flag and the OCR1 are undeterminate at power-on and are not affected by an external reset, care must be exercise when initiating the output compare function with software. The following procedure is recommended to prevent the OCF1 flag from being set between the time it is read and the write to OCR1:

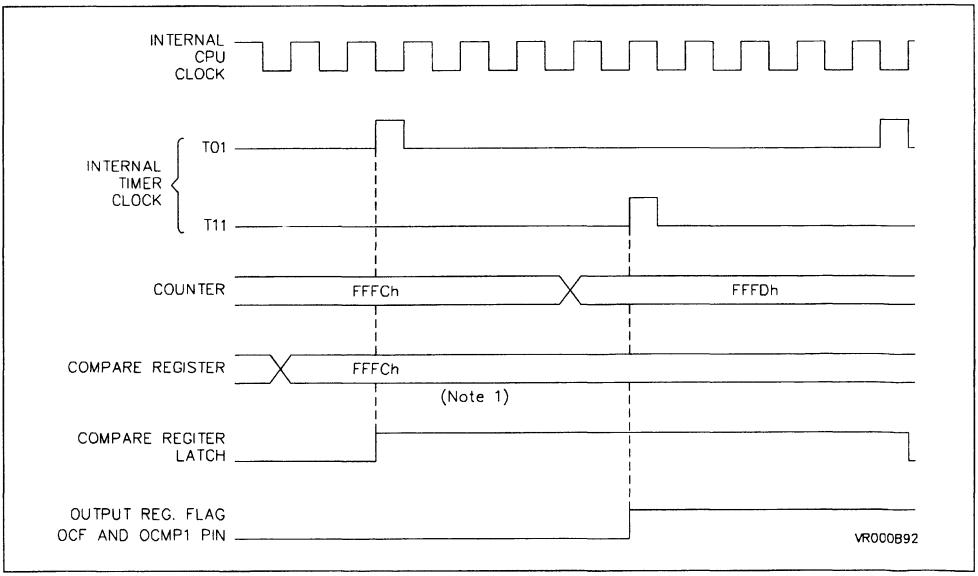
Write to OCHR1 (further compares are inhibited).

Read the TSR (first step of the clearance of OCF1 [it may be already set]).

Write to OCLR1 (enables the output compare function and clears OCF1).

Output Compare Register 2. The Output Compare Register 2 (OCR2) is a 16-bit register, which is made up of two 8-bit registers: the most significant byte register (OCHR2) at address 001Eh and

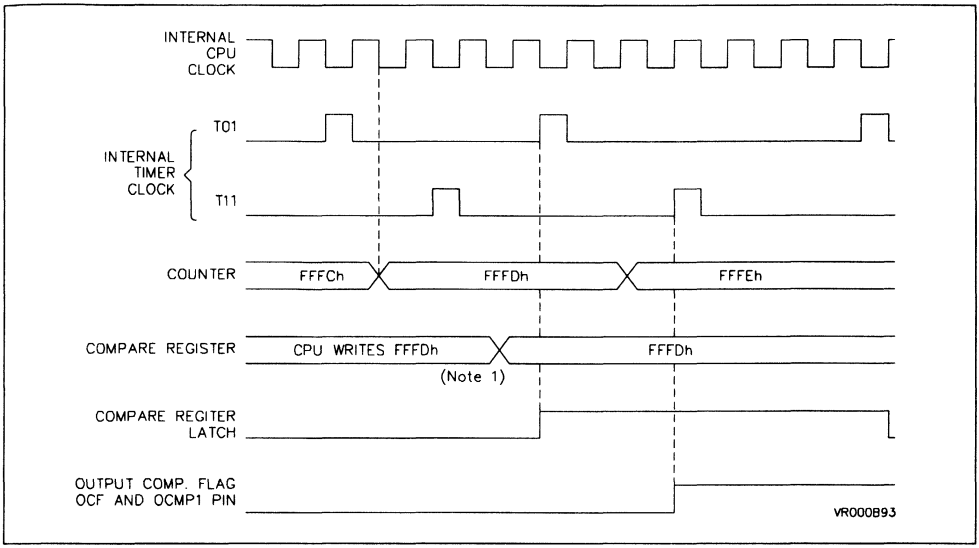
Figure 20. Ouput Compare Timing Diagram Slow Mask Option



Note 1: The CPU write to the compare registers may take place at any time but a compare only occurs at timer state T01. Thus an 8-cycle difference may exist between the write to the compare register and the actual compare.

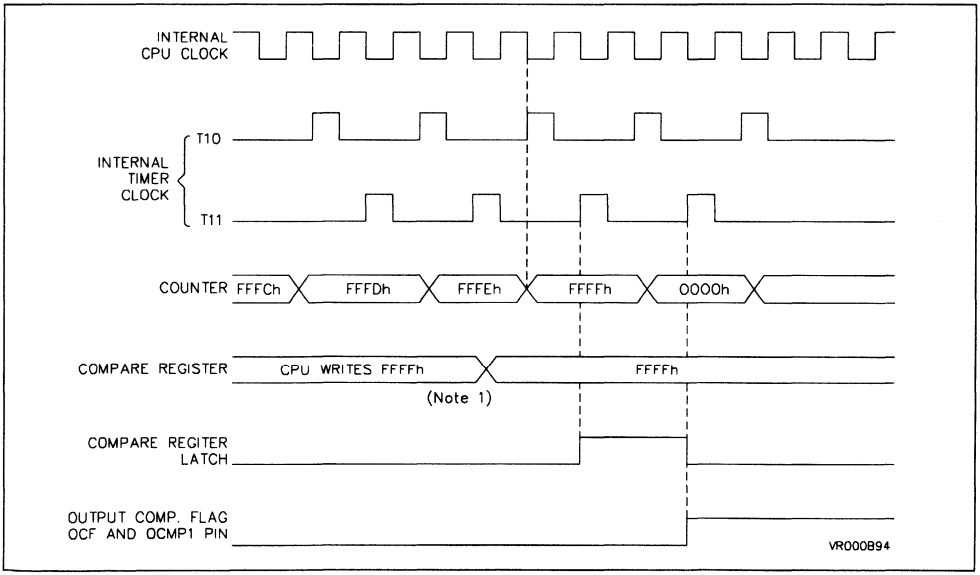
16 BIT TIMER (Continued)

Figure 21. Output Compare Timing Diagram Standard Mask option



Note 1: The CPU write to the compare registers may take place at any time but a compare only occurs at timer state T01. Thus a 4-cycle difference may exist between the write to the compare register and the actual compare.

Figure 22. Output Compare Timing Diagram Fast Mask Option



Note 1: The CPU write to the compare registers may take place at any time but a compare only occurs at timer state T11. Thus a 2-cycle difference may exist between the write to the compare register and the actual compare.

16 BIT TIMER (Continued)

the least significant byte register (OCLR2) at address 001Fh.

This register works as the Output Compare Register 1. For a complete description, please, refer above in substituting the appropriate index in the bit and register names.

Software Force Compare. The force compare capability main purpose is to facilitate fixed frequency generation.

When the Force Output Level 1 bit (FOLV1) of TCR is written to 1, OLVL1 is copied to pin OCMP1. To provide this capability, internal logic allows a single instruction to change OLVL1 and causes a forced compare with the new value of OLVL1. OCF1 is not affected and thus, no interrupt request is generated.

2.3.2 Timer Registers

TIMER CONTROL REGISTER (0012h)

Read/Write
Reset Value: 0000 00X0 (00h or 02h)

The TCR is an 8 bit read/write register. Its eight bits are defined as follow:

7							0
ICIE	OCIE	TOIE	—	FOLV1	—	IEDG1	OLVL1

Bit 7 = **ICIE** *Input Capture Interrupt Enable*
If ICIE is set, a timer interrupt is enabled whenever the ICF1 status flags of TSR are set. If the ICIE bit is cleared, the interrupt is inhibited.

Bit 6 = **OCIE** *Output Compare Interrupt Enable*
If OCIE is set, a timer interrupt is enabled whenever the OCF1 or OCF2 status flags of TSR are set. If the OCIE bit is cleared, the interrupt is inhibited.

Bit 5 = **TOIE** *Timer Overflow Interrupt Enable*
If TOIE is set, a timer interrupt is enable whenever the TOF status flag of TSR is set. If the TOIE bit is cleared, the interrupt is inhibited.

Bit 4 = Unused

Bit 3 = **FOLV1** *Force Output Compare 1*
When written to 1, FOLV1 forces OLVL1 to be copied to the OCMP1 pin. FOLV1 has no effect otherwise. It can only be reset by a system reset.

Bit 2 = Unused

Bit 1 = **IEDG1** *Input Edge 1*
The value of the IEDG1 determines which level transition on pin ICAP will trigger a free running counter transfer to the ICR1. When IEDG1 is high, a rising edge triggers the capture since when low, a falling edge does.

Bit 0 = **OLVL1** *Output Level 1*
The OLVL1 bit is copied to the OCMP1 pin whenever a successful comparison occurs at OCR1.

TIMER STATUS REGISTER (0013h)

Read Only
Reset Value: Undefined

The Timer Status Register (TSR) is an 8-bit register of which the five most significant bits contain read-only status information and the three least significant bits are not used.

7							0
ICF1	OCF1	TOF	—	OCF2	—	—	—

Bit 7 = **ICF1** *Input Capture Flag 1*
ICF1 is set when a proper edge has been sensed by the input capture edge detector at pin ICAP. The edge is selected by the IEDG1-bit in TCR. ICF1 is cleared by a processor access to the TSR while ICF1 is set followed by an access (read or write) to the low byte of ICR1 (ICLR1).

Bit 6 = **OCF1** *Output Compare Flag 1*
OCF1 is set when the content of the free running counter matches the content of OCR1. It is cleared by a processor access of TSR while OCF1 is set followed by an access (read or write) to the low byte of OCR1.

Bit 5 = **TOF** *Timer Overflow*
TOF is set by a transition of the free running counter from FFFFh to 0000h. It is cleared by a processor access to TSR while TOF is set followed by an access (read or write) to the low byte of the counter low register. TOF is not affected by an access to the Alternate Counter Register.

Bit 4 = Unused

Bit 3 = **OCF2** *Output Compare Flag 2*
OCF2 is set when the content of the free running counter matches the content of OCR2. It is cleared by a processor access of TSR while OCF2 is set followed by an access (read or write) to the low byte of OCR2.

Bit 2, 1, 0 = Unused.

3 SOFTWARE AND CHARACTERISTICS

3.1 SOFTWARE DESCRIPTION

3.1.1 Instruction Set

The ST7 instruction set is an 8 bit industry standard instruction set that can be divided into five major groups. All instructions of each group have the same addressing modes.
Refer to ST7 MACRO ASSEMBLER USER'S GUIDE and ST7 PROGRAMMING MANUAL for detailed information.

Group 1 : Register/Memory And Absolute Jump Group In this group most instructions contain two operands. One operand is inherently defined as either the accumulator or an index register. The other operand is fetched from memory using one of the allowed addressing modes. The absolute jump instructions are included in this group because they can use most of the addressing modes of the register/memory instructions.

Examples: LD <ea>, a. This means that the memory byte located at address <ea> is loaded with the 8-bit content of the accumulator A.

The list of the instructions of this group is given in Table 8.

Group 2 : Read - Modify - Write Group These instructions read a register or a memory location, modify its content and write the new value back.

Example : RRC <ea>. This means that the content of the memory byte located at address <ea> is rotated right through the carry bit, the result is written in the memory <ea> and the carry bit.

The list of the instructions of this group is given in Table 9.

Group 3 : Bit Manipulation And Test Group Bit manipulation instructions can set or clear any bit within the first 256 memory locations, except for ROM (020h - 04F) and read-only registers located at addresses 03h, 0Bh, 010h, 013h, 014h and 015h.

Example: BSET <ea>, #b. This sets the bit #b of memory location <ea>.

Test instructions can test any bit of the first 256 memory locations and jump conditional within an 8 bit PC-relative displacement.

Example: BTJT <ea>, #b, ee. This corresponds to the relative jump (displacement = ee) if bit number #b of memory location <ea> is set. (Bit test and jump if true).

The list of the instructions of this group is given in Table 10.

Group 4 : PC-Relative Jump Group These instructions execute a PC-relative jump (8-bit displacement) depending on the state of the flag bits inside the condition code register (H, I, N, Z, C flags).

Example: JRC ee. This means jump with displacement ee from actual the PC value if the carry bit is set, else execute the next instruction.

The list of the instructions of this group is given in Table 11.

Group 5 : Miscellaneous Group These instructions are mainly control instructions on registers, stack, interrupts, subroutines and power down modes.

The multiply instruction is included in this group. It performs an 8 x 8 bit unsigned multiplication between one index register and the accumulator. The result is given as 16 bits, with the high order byte in the index register and the low order one in the accumulator.

The list of the instructions of this group is given in Table 12.

3.1.2 Addressing Modes

The CPU uses 9 main addressing modes to provide the programmer with an opportunity to optimize his code in most applications.

The various indexed addressing modes make it possible to locate data labels, code conversion tables and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions, while the longest instructions (three bytes) allow access of tables throughout memory.

Short absolute (direct) and long absolute (extended) addressing modes are also included. Extended addressing permits jump instructions to reach all memory.

The various addressing modes differ from each other in computing the effective address (EA) i.e. in calculating the address to or from which the argument of an instruction is fetched or stored. The LSBEA is the least significant byte of the EA; the MSBEA is its most significant byte. The 17 addressing modes of the processor are described below.

The table of symbols is given in Table 9 while the effective address coding is given in Table 8.

SOFTWARE DESCRIPTION (Continued)

In order to extend the number of op-codes available for an eight bit CPU (256 op-codes), three "pre-byte" op-codes have been defined. These pre-byte have to be seen as pre-instructions that modify the meaning of the instruction they precede. The whole instruction becomes:

PC-1 End of previous instruction

PC Pre-byte

PC + 1 Op-code

PC + 2 Additional word (0 to 2) according to the number of byte required to compute the effective address.

The pre-bytes enable instructions in Y as well as indirect addressing modes to be implemented. They precede the opcode of the instruction in X or of the instruction using a direct addressing mode.

The pre-bytes are :

PDY : 90h Transform an instruction in X using immediate, direct, indexed, direct bit or inherent addressing modes to an instruction in Y using the same addressing mode.

PIY : 91h Transform an instruction using X indexed addressing mode to an instruction using indirect Y indexed addressing mode.

PIX : 92h Transform an instruction using direct, direct bit or direct relative addressing mode to an instruction using the corresponding indirect addressing mode. It also transforms an instruction using X indexed addressing mode to an instruction using indirect X indexed addressing mode.

The pre-byte is completely user transparent. It is part of the assembly code.

Table 8. Source Coding

Addressing Mode	Source Coding	Example
Immediate	#nn	LD a, #0Ah
Direct	ad8	LD a, 0Ah
Extended	ad16	LD a, 10EAh
Indexed no offset	(iX)	LD a, (X)
Indexed 8 bit offset	(d8, iX)	LD a, (1Bh, Y)
Indexed 16 bit offset	(d16, iX)	LD a, (100Ah, X)
Memory indirect short	[ad8]	LD a, [1Bh]
Memory indirect long	[ad16]	LD a, [100Ah]
Memory indirect short indexed	([ad8], iX)	LD a, ([1Bh], X)
Memory indirect long indexed	([ad16], iX)	LD a, ([100Ah], Y)

Table 9. Table of Symbols

a	Accumulator	nn	8 bit immediate value
iX	Index register (either X o r Y)	ad8	8 bit address
X	X index register	ad16	16 bit address
Y	Y index register	d8	8 bit signed offset
S	Stack pointer	d16	16 bit signed offset
CC	Condition code register	ee	8 bit PC relative displacement
<ea>	Effective address	b	3 bit number

SOFTWARE DESCRIPTION (Continued)

The addressing modes are discussed in the following paragraphs.

Inherent. In inherent instructions, there is no EA as there is no operand to fetch or store. All the information needed to execute the instruction is contained in the op-code. Operations specifying only an index register or the accumulator, and no other arguments, are included in this mode.

Immediate. In immediate addressing the operand is stored in the byte immediately following the op-code.

Direct Modes

Direct. In the direct addressing mode, the effective address is contained in a single byte following the op-code byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction.

Extended. In the extended addressing mode, the effective address of the argument is contained in the two bytes following the op-code. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory.

Indexed Modes

Indexed Without Offset. In the indexed without offset addressing mode, the effective address is contained in one index register (X or Y). This addressing mode can therefore access the first 256 memory locations. These instructions are only one byte long.

This mode is mainly used to move a pointer through a table or to address a frequently referenced RAM or I/0 location.

Indexed 8 Bit Offset. The EA is obtained by adding the 8-bit unsigned contents of the second instruction byte to the 8-bit unsigned content of the appropriate index register. This mode allows addressing of 256 locations of the 511 lowest memory locations.

Indexed 16 Bit Offset. The EA is obtained by adding the 16-bit unsigned value composed of the second (MSB) and the third (LSB) instruction bytes to the 8-bit unsigned content of the appropriate **index register**. This mode allows addressing of 256 locations anywhere in the memory map.

Indirect Modes

Short Indirect. In this mode, the second byte of the instruction is used as a page zero address. The content of this page zero memory location is the LSB of the effective address. The MSBEA is zero (i.e. the effective address points to a page zero location).

Long Indirect. In the long indirect mode, the second byte of the instruction is used as a page zero pointer. The MSBEA is the content of this location while the LSBEA is the content of the following page zero location.

Indirect Indexed Modes

Short Indirect Indexed. The second byte of the instruction is used as a page zero address. To obtain the LSBEA, the content of this page zero memory location is added to the 8- bit unsigned value contained in the specified index register. The MSBEA is zero (i.e. the effective address points to a page zero location).

Long Indirect Indexed. In long indirect indexed mode, the second byte of the instruction is used as a page zero pointer. The 16-bit word read from this location (MSB at the pointed address and LSB at the following one) is added to the 8-bit unsigned value contained in the specified index register to form the 16-bit EA.

Relative Modes

Simple Relative. The relative addressing mode is used for branch instruction (e.g. Branch on bit, Branch on condition, Branch subroutine). The branch address (new value of PC) is calculated by adding a displacement given by the 8-bit signed byte following the op-code value to the actual content of the PC. This means that the variation of PC value is in the range -126 to +129 from the op-code address (the offset value can be calculated by the assembler).

Indirect Relative. The indirect relative addressing mode is similar to the relative mode but the content of the second byte of the instruction is used as a page zero address containing the 8-bit signed displacement value to be added to the actual content of the PC (i.e. address of the op-code plus 2).

SOFTWARE DESCRIPTION (Continued)

Direct Bit Modes

Bit Set And Clear. Bit Set/Clear mode is used to read-modify-write one single bit of a memory location in page zero, including I/O bits. The concerned memory location is given by the byte following the op-code (direct addressing mode) while the position of the bit to deal with is given in 3 bits included in the op-code.

Bit Test And Branch. Bit test and branch mode gives a relative branch according to the value of a single bit of a memory location in page zero. The op-code contains 3 bits to define the bit to test at a location given by the byte immediately following the op-code. A third byte gives the 8-bit signed value of the PC-relative displacement. If the test is true, this displacement is added to the actual content of the PC (i.e. op-code address plus 2) to form the new value of the PC.

Indirect Bit Modes

Indirect Bit Set And Clear. Indirect Bit Set/Clear mode works similarly to the bit Set/Clear mode except that the address of the concerned byte is the content of the location pointed by the second byte of the instruction.

Indirect Bit Test And Branch. This mode works as the bit test and branch mode but the tested byte is the content of the location pointed by the second byte of the instruction.

SOFTWARE DESCRIPTION (Continued)

Example

FUNCTION	SOURCE CODING	ADDRESSING MODES
		Immediate
Load a with memory	LD a,<ea >	$_2$A6 ^{2}

# Bytes	OP-Code	# Cycles

Table 10. Register/Memory and Absolute Jump Group

FUNCTION	SOURCE CODE	ADDRESSING MODE					
		Immediate	Direct	Extended	Index 0	Index 8	Index 16
Load A with memory	LD a,<ea>	$_2$A6 ^{2}	$_2$B6 ^{3}	$_3$C6 ^{4}	$_1$F6 ^{3}	$_2$E6 ^{4}	$_3$D6 ^{5}
Load iX with memory	LD iX,<ea>	$_2$AE ^{2}	$_2$BE ^{3}	$_3$CE ^{4}	$_1$FE ^{3}	$_2$EE ^{4}	$_3$DE ^{5}
Load memory with A	LD <ea>,a	—	$_2$B7 ^{4}	$_3$C7 ^{5}	$_1$F7 ^{4}	$_2$E7 ^{5}	$_3$D7 ^{6}
Load memory with iX	LD <ea>,iX	—	$_2$BF ^{4}	$_3$CF ^{5}	$_1$FF ^{4}	$_2$EF ^{5}	$_3$DF ^{6}
Add memory to A	ADD a,<ea>	$_2$AB ^{2}	$_2$BB ^{3}	$_3$CB ^{4}	$_1$FB ^{3}	$_2$EB ^{4}	$_3$DB ^{5}
Add memory and carry to A	ADC a,<ea>	$_2$A9 ^{2}	$_2$B9 ^{3}	$_3$C9 ^{4}	$_1$F9 ^{3}	$_2$E9 ^{4}	$_3$D9 ^{5}
Subtract memory to A	SUB a,<ea>	$_2$A0 ^{2}	$_2$B0 ^{3}	$_3$C0 ^{4}	$_1$F0 ^{3}	$_2$E0 ^{4}	$_3$D0 ^{5}
Subtract memory with carry	SBC a,<ea>	$_2$A2 ^{2}	$_2$B2 ^{3}	$_3$C2 ^{4}	$_1$F2 ^{3}	$_2$E2 ^{4}	$_3$D2 ^{5}
And memory to A	AND a,<ea>	$_2$A4 ^{2}	$_2$B4 ^{3}	$_3$C4 ^{4}	$_1$F4 ^{3}	$_2$E4 ^{4}	$_3$D4 ^{5}
Or memory with A	OR a,<ea>	$_2$AA ^{2}	$_2$BA ^{3}	$_3$CA ^{4}	$_1$FA ^{3}	$_2$EA ^{4}	$_3$DA ^{5}
Exclusive OR	XOR a,<ea>	$_2$A8 ^{2}	$_2$B8 ^{3}	$_3$C8 ^{4}	$_1$F8 ^{3}	$_2$E8 ^{4}	$_3$D8 ^{5}
Arithmetic Compare A	CP a,<ea>	$_2$A1 ^{2}	$_2$B1 ^{3}	$_3$C1 ^{4}	$_1$F1 ^{3}	$_2$E1 ^{4}	$_3$D1 ^{5}
Arithmetic Compare iX	CP iX,<ea>	$_2$A3 ^{2}	$_2$B3 ^{3}	$_3$C3 ^{4}	$_1$F3 ^{3}	$_2$E3 ^{4}	$_3$D3 ^{5}
Bit compare A and memory	BCP a,<ea>	$_2$A5 ^{2}	$_2$B5 ^{3}	$_3$C5 ^{4}	$_1$F5 ^{3}	$_2$E5 ^{4}	$_3$D5 ^{5}
Absolute Jump	JP <ea>	—	$_2$BC ^{2}	$_3$CC ^{3}	$_1$FC ^{2}	$_2$EC ^{3}	$_3$DC ^{4}
Call subroutine	CALL <ea>	—	$_2$BD ^{5}	$_3$CD ^{6}	$_1$FD ^{5}	$_2$ED ^{6}	$_3$DD ^{7}

SOFTWARE DESCRIPTION (Continued)

Table 11. Read - Modify - Write Group

FUNCTION	SOURCE CODE	ADDRESSING MODE						
		Inh a	Inh iX	Direct	Memory Direct	Index 0	Index +d8	Index +[ad8]
Increment	INC <ea>	$_1$4C ^{3}	$_1$5C ^{3}	$_2$3C ^{5}	$_3$923C ^{7}	$_1$7C ^{5}	$_2$6C ^{6}	$_3$926C ^{8}
(Y index)			$_2$905C ^{4}		$_3$913C ^{7}	$_2$907C ^{6}	$_3$906C ^{7}	$_3$916C ^{8}
Decrement	DEC <ea>	$_1$4A ^{3}	$_1$5A ^{3}	$_2$3A ^{5}	$_3$923A ^{7}	$_1$7A ^{5}	$_2$6A ^{6}	$_3$926A ^{8}
(Y index)			$_2$905A ^{4}			$_2$907A ^{6}	$_3$906A ^{7}	$_3$916A ^{8}
Clear	CLR <ea>	$_1$4F ^{3}	$_1$5F ^{3}	$_2$3F ^{5}	$_3$923F ^{7}	$_1$7F ^{5}	$_2$6F ^{6}	$_3$926F ^{8}
(Y index)			$_2$905F ^{4}			$_2$907F ^{6}	$_3$906F ^{7}	$_3$916F ^{8}
One's Complement	CPL <ea>	$_1$43 ^{3}	$_1$53 ^{3}	$_2$33 ^{5}	$_3$9233 ^{7}	$_1$73 ^{5}	$_2$63 ^{6}	$_3$9263 ^{8}
(Y index)			$_2$9053 ^{4}			$_2$9073 ^{6}	$_3$9063 ^{7}	$_3$9163 ^{8}
Negate (2's complement)	NEG <ea>	$_1$40 ^{3}	$_1$50 ^{3}	$_2$30 ^{5}	$_3$9230 ^{7}	$_1$70 ^{5}	$_2$60 ^{6}	$_3$9260 ^{8}
(Y index)			$_2$9050 ^{4}			$_2$9070 ^{6}	$_3$9060 ^{7}	$_3$9160 ^{8}
Rotate Left thru Carry	RLC <ea>	$_1$49 ^{3}	$_1$59 ^{3}	$_2$39 ^{5}	$_3$9239 ^{7}	$_1$79 ^{5}	$_2$69 ^{6}	$_3$9269 ^{8}
(Y index)			$_2$9059 ^{4}			$_2$9079 ^{6}	$_3$9069 ^{7}	$_3$9169 ^{8}
Rotate Right thru Carry	RRC <ea>	$_1$46 ^{3}	$_1$56 ^{3}	$_2$36 ^{5}	$_3$9236 ^{7}	$_1$76 ^{5}	$_2$66 ^{6}	$_3$9266 ^{8}
(Y index)			$_2$9056 ^{4}			$_2$9076 ^{6}	$_3$9066 ^{7}	$_3$9166 ^{8}
Shift Left Logical	SLL <ea>	$_1$48 ^{3}	$_1$58 ^{3}	$_2$38 ^{5}	$_3$9238 ^{7}	$_1$78 ^{5}	$_2$68 ^{6}	$_3$9268 ^{8}
(Y index)			$_2$9058 ^{4}			$_2$9078 ^{6}	$_3$9068 ^{7}	$_3$9168 ^{8}
Shift Right Logical	SRL <ea>	$_1$44 ^{3}	$_1$54 ^{3}	$_2$34 ^{5}	$_3$9234 ^{7}	$_1$74 ^{5}	$_2$64 ^{6}	$_3$9264 ^{8}
(Y index)			$_2$9054 ^{4}			$_2$9074 ^{6}	$_3$9064 ^{7}	$_3$9164 ^{8}
Shift Left Arithmetic	SLA <ea>	$_1$48 ^{3}	$_1$58 ^{3}	$_2$38 ^{5}	$_3$9238 ^{7}	$_1$78 ^{5}	$_2$68 ^{6}	$_3$9268 ^{8}
(Y index)			$_2$9058 ^{4}			$_2$9078 ^{6}	$_3$9068 ^{7}	$_3$9168 ^{8}
Shift Right Arithmetic	SRA <ea>	$_1$47 ^{3}	$_1$57 ^{3}	$_2$37 ^{5}	$_3$9237 ^{7}	$_1$77 ^{5}	$_2$67 ^{6}	$_3$9267 ^{8}
(Y index)			$_2$9057 ^{4}			$_2$9077 ^{6}	$_3$9067 ^{7}	$_3$9167 ^{8}
Test for Negative or Zero	TNZ <ea>	$_1$4D ^{3}	$_1$5D ^{3}	$_2$3D ^{4}	$_3$923D ^{6}	$_1$7D ^{4}	$_2$6D ^{5}	$_3$926D ^{7}
(Y index)			$_2$905D ^{4}			$_2$907D ^{5}	$_3$906D ^{6}	$_3$916D ^{7}
Swap Nibbles	SWAP <ea>	$_1$4E ^{3}	$_1$5E ^{3}	$_2$3E ^{5}	$_3$923E ^{7}	$_1$7E ^{5}	$_2$6E ^{6}	$_3$926E ^{8}
(Y index)			$_2$905E ^{4}			$_2$907E ^{6}	$_3$906E ^{7}	$_3$916E ^{8}

SOFTWARE DESCRIPTION (Continued)

Table 12. Bit Manipulation And Test Group

FUNCTION	SOURCE CODE	ADDRESSING MODES	
		Relative	Indirect Relative
Bit Set	BSET < ea > , # b	2 (10+2*b) [5]	3 92(10+2*b) [7]
Bit Reset	BRES < ea > , # b	2 (11+2*b) [5]	3 92(10+2*b) [7]
Bit Test and Jump if True	BTJT < ea > , # b , ee	3 (00+2*b) [5]	4 92(00+2*b) [7]
Bit Test and Jump if False	BTJF < ea > , # b , ee	3 (01+2*b) [5]	4 92(01+2*b) [7]

Table 13. PC-Relative Jump Group

FUNCTION	SOURCE CODE	ADDRESSING MODES	
		Relative	Indirect Relative
Jump Relative True	JRT ee	2 20 [3]	3 9220 [5]
(Jump Relative always)	JRA ee	2 20 [3]	3 9220 [5]
Jump Relative False	JRF ee	2 21 [3]	3 9221 [5]
Jump Relative if Unsigned Greater than	JRUGT ee	2 22 [3]	3 9222 [5]
Jump Relative if Unsigned Lower or Equal	JRULE ee	2 23 [3]	3 9223 [5]
Jump Relative if No Carry	JRNC ee	2 24 [3]	3 9224 [5]
Jump Relative if Unsigned Greater or Equal	JRUGE ee	2 24 [3]	3 9224 [5]
Jump Relative if Carry	JRC ee	2 25 [3]	3 9225 [5]
Jump Relative if Unsigned Lower than	JRULT ee	2 25 [3]	3 9225 [5]
Jump Relative if Not Equal	JRNE ee	2 26 [3]	3 9226 [5]
Jump Relative if Equal	JREQ ee	2 27 [3]	3 9227 [5]
Jump Relative if Half Carry	JRH ee	2 28 [3]	3 9228 [5]
Jump Relative if Not Half Carry	JRNH ee	2 29 [3]	3 9229 [5]
Jump Relative if Plus	JRPL ee	2 2A [3]	3 922A [5]
Jump Relative if Minus	JRMI ee	2 2B [3]	3 922B [5]
Jump Relative if Not Interrupt Mask	JRNM ee	2 2C [3]	3 922C [5]
Jump Relative if Interrupt Mask	JRM ee	2 2D [3]	3 922D [5]
Jump Relative if Interrupt Line Low	JRIL ee	2 2E [3]	3 922E [5]
Jump Relative if Interrupt Line High	JRIH ee	2 2F [3]	3 922F [5]
Call Subroutine Relative	CALLR ee	2 AD [6]	3 92AD [8]

SOFTWARE DESCRIPTION (Continued)

Table 14. Miscellaneous Group

FUNCTION	SOURCE CODE	X iNDEX
Multiply (iX, A = iX * A)	MUL iX,a	1 42 [11]
Load iX with acc. a content	LD iX,a	1 97 [2]
Load a with iX content	LD a,iX	1 9F [2]
Load Stack p. with acc. a content	LD S,a	1 95 [2]
Load acc. a with Stack p. content	LD a,S	1 9E [2]
Load Stack p. with iX content	LD S,iX	1 94 [2]
Load iX with Stack p. content	LD iX,S	1 96 [2]
Load X // with Y // content	LD X,Y	1 93 [2]
Load Y // with X // content	LD Y,X	—
Push acc. a onto the Stack	PUSH A	1 88 [3]
Pop acc. a from the Stack	POP A	1 84 [4]
Push iX onto the stack	PUSH iX	1 89 [3]
Pop iX from the Stack	POP iX	1 85 [4]
Push Condition Codes onto the Stack	PUSH CC	1 8A [3]
Pop Condition Codes from the Stack	POP CC	1 86 [4]
Reset Carry Flag	RCF	1 98 [2]
Set Carry Flag	SCF	1 99 [2]
Reset Interrupt Mask	RIM	1 9A [2]
Set Interrupt Mask	SIM	1 9B [2]
Reset Stack Pointer	RSP	1 9C [2]
No Operation	NOP	1 9D [2]
Interrupt Routine Return	IRET	1 80 [9]
Subroutine Return	RET	1 81 [6]
Software Trap	TRAP	1 83 [10]
Halt	HALT	1 8E [2]
Wait For Interrupt	WFI	1 8F [2]

3.2 ELECTRICAL CHARACTERISTICS

Power considerations

T_J, the average chip-junction temperature in Celsius can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta JA) \quad (1)$$

Where:

- T_A is the Ambient Temperature in °C,
- θJA ithe Package Thermal Resistance, Junction-to-Ambient in °C/W,
- P_D the sum of P_{INT} and $P_{I/O}$,
- P_{INT} equals I_{CC} time V_{CC}, Watts-Chip Internal Power
- $P_{I/O}$ the Power Dissipation on Input and Output Pins, User Determined.

For most applications $P_{I/O} < P_{INT}$ and can be neglected .

P_{PORT} may be significant if the device is configured to drive Darlington bases or sink LED Loads.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Therefore :

$$K = P_D \times (T_A + 273°C) + \theta JA \times P_D^2 \quad (3)$$

Where K is constant pertaining to the particular part, K can be determined from equation (3) by measuring P_D (at equilibrium) for a kwon T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

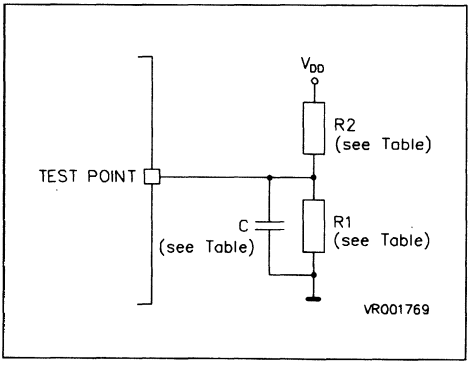
Thermal Characteristics

Symbol	Characteristics	Value	Unit
θJA	Thermal Resistance PDIP28 PSO28	 47 50	°C/W

Equivalent Test Load

V_{DD} = 3V			
Pins	**R1**	**R2**	**C**
PA0-PA7	10.91kΩ	6.32kW	50pF
PB0-PB7	10.91kΩ	6.32kW	50pF
PC0-PC5	10.91kΩ	6.32kW	50pF
V_{DD} = 4.5V			
Pins	**R1**	**R2**	**C**
PA0-PA7	3.26kΩ	2.38kW	50pF
PB0-PB7	3.26kΩ	2.38kW	50pF
PC0-PC5	3.26kΩ	2.38kW	50pF

Test Diagram



AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD}	Operating Supply Voltage	RUN Mode HALT Mode EEPROM Write EEPROM Read	2.5 2.0 3.0 2.5		5.5	V
I_{DD}	Supply Current [1]	RUN Mode V_{DD}=5V,f_{OSC}=4MHz V_{DD}=2.5V,f_{OSC}=1MHz V_{DD}=3.5V,f_{OSC}=455KHz WAIT Mode V_{DD}=5V,f_{OSC}=4MHz V_{DD}=2.5V.f_{OSC}=1MHz V_{DD}=3.5V,f_{OSC}=455KHz EEPROM Programming V_{DD}=5V,f_{OSC}=4MHz V_{DD}=3.5V,f_{OSC}=455KHz HALT Mode V_{DD}=5V,T_A=70°C		 1.8 0.9 1	 2.5 0.4 0.7 1.5 200 500 2.5 0.5 10	 mA mA mA mA µA µA mA mA µA
V_{OL}	Ouput Low Voltage	Port A, B - Open Drain I_{LOAD} =200µA			0.1xV_{DD}	V

Note 1. Measured with a quartz for the 1 or 4MHz Frequency or with a ceramic resonator for 455KHz Frequency.

DC Electrical Characteristics

(V_{DD} = 5.0V±10%, V_{SS} = 0V, T_A = operating temperature range, unless otherwise noted)

Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Output Voltage, Load ≤ 10.0µA			0.1	V
V_{OH}		V_{DD}-0.1			V
V_{OH}	Output High Voltage I LOAD = 0.8mA, PA0-PA7,PB0-PB7,PC0-PC5	V_{DD}-0.8			V
V_{OL}	Output Low Voltage (I LOAD = 1.6 mA) PA0-PA7,PB0-PB5,PC0-PC5,$\overline{RESET}$			0.4	V
V_{IH}	Input High Voltage PA0-PA7,PB0-PB7,PC0-PC5,$\overline{INT}$,$\overline{RESET}$	0.7xV_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage PA0-PA7,PB0-PB7,PC0-PC5,$\overline{INT}$, $\overline{RESET}$	V_{SS}		0.2xV_{DD}	V
V_{RM}	Data Retention Mode (0 to 70°C)	2			V
I_{IL}	I/O Ports Hi-Z Leakage Current PA0-PA7,PB0-PB7,PC0-PC5			± 10	µA
I_{IN}	Input Current : $\overline{RESET}$, $\overline{INT}$, ICAP			± 1	µA
C_{OUT}	Capacitance : Ports (as Input or Output)			12	pF
C_{IN}	$\overline{RESET}$, $\overline{INT}$, ICAP			8	pF

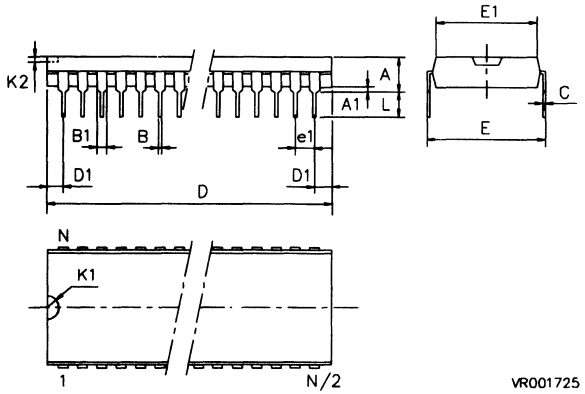
Control Timing

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Frequency of Operation	V_{DD}=5V V_{DD}=3V V_{DD}=2.5V	DC DC DC		4 2 1	MHz
t_{ILCH}	HALT Mode Recovery Startup Time	Ceramic resonator			20	ms
t_{RL}	External RESET Input Pulse Width		1.5			t_{CYC}
t_{PORL}	Power RESET Ouput		4096			t_{CYC}
t_{DOGL}	Watchdog RESET Output Pulse Width		1.5			t_{CYC}
t_{DOG}	Watchdog Time-out		6144		7168	t_{CYC}
t_{PROG}	EEPROM Programming Time (0 to 70)			2	8	ms
t_{ILIH}	Interrupt Pulse Width INT PORTC		 125 125			ns
t_{ILIL}	Interrupt Pulse Period		(1)			t_{CYC}
t_{DDR}	Power up rise time	V_{DDmin}			100	ms

Note 1. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 cycles.

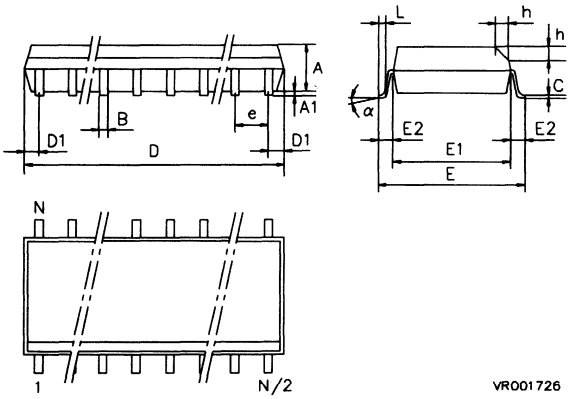
3.3 PACKAGE MECHANICAL DATA

Figure 23. 28-Plastic Dual In line Package, 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		4.8	0.086		0.189
A1	0.51		1.77	0.010		0.069
B	0.38		0.58	0.015		0.023
B1	0.97		1.52	0.055		0.065
C	0.2		0.3	0.008		0.009
D	35.06		36.22	1.400		1.425
D1	–	–	–	–	–	–
E			16.3			0.641
E1		12.9				0.508
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	3.18		4.44	1.25		0.174
e1		2.54			0.10	
Number of Pins						
N	28					

Figure 24. 28-Lead Small Outline Plastic, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	17.7		18.1	.6969		.7125
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	28					

3.4 ORDERING INFORMATION

Ordering Information Table

Sales Types	Memory Type	Temperature Range	Package
ST7294B1 ST7294M1	6K ROM	-0 to + 70°C	PDIP28 PSO28
ST7294B8 ST7294M8	6K ROM	-25 to + 85°C	PDIP28 PSO28

ST7294 MICROCONTROLLER OPTION LIST

Customer: .....
Address: .....
Contact: .....
Phone No: .....
Reference: .....

SGS-THOMSON Microelectronics references

Package	[ ] Plastic Dual in Line	[ ] Plastic Small Outline
Temperature Range	[ ] 0 to 70°C	[ ] -25 to 85°C
Software Development	[ ] Customer	[ ] SGS-THOMSON
	[ ] External Laboratory	

For marking one line with 11 characters maximum is possible
Special Marking [ ] (y/n) "_ _ _ _ _ _ _ _ _ _ _" Letters, digits, ' . ', ' - ', ' / ' and spaces only

OPTION LIST:

TIMER CLOCK	[ ] STANDARD ($f_{OP}/4$) [ ] FAST ($f_{OP}/2$) [ ] SLOW ($f_{OP}/8$)
Watchdog ENABLE MODE	[ ] Software Enable [ ] Auto Enable
Watchdog during WAIT	[ ] Active during WAIT mode [ ] Suspend during WAIT mode
Enable Wake-up on PORTC	[ ] PORTC 6-bit I/O PORT [ ] PORTC interrupt Wake-up inputs
Pinout for ICAP (PC0)	[ ] ICAP is bonded on pin 18 [ ] PC0 is bonded on pin 18
Pinout for OCMP1 (PC1)	[ ] OCMP1 is bonded on pin 17 [ ] PC1 is bonded on pin 17
PORT A Outputs	[ ] Standard push-pull output PORT [ ] Open Drain output PORT
PORT A Pull-up	[ ] No pull-up [ ] Pull-up when a line is defined as an Input
PORT B Pull-up	[ ] No pull-up [ ] Pull-up when a line is defined as an Input

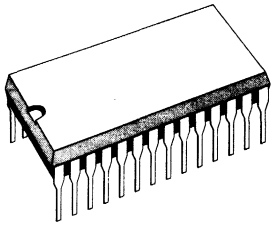
Signature .....

Date .....

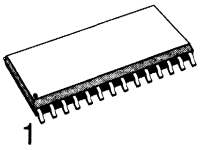
8-BIT EPROM HCMOS MCUs WITH EEPROM

PRELIMINARY DATA

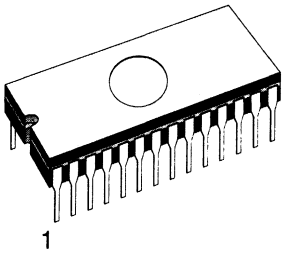
- 3V to 5.5V supply operating range
- 4MHz Maximum Clock Frequency
- Fully static operation
- -25 to +85°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention Modes
- User EPROM: 7168 bytes
  Data RAM: 224 bytes
  EEPROM: 256 bytes
- 28-pin Plastic Dual In Line and SO package for ST72T94 OTP version
- 28-pin Ceramic Dual In Line package for ST72E94 EPROM version
- 22 bidirectional I/O lines
- 6 lines programmable as interrupt wake-up inputs
- 16-bit timer with 1 input capture and 2 output compares
- 2V RAM retention mode
- Master Reset and power on reset
- Full Hardware Emulator
- Compatible with ST7294 (6K) and ST7293 (3.3K) ROM devices
- 8-bit data manipulation
- 74 basic instructions
- 10 main addressing modes
- 8x8 unsigned multiply instruction
- true bit manipulation
- Complete development support on real time emulator with PC/DOS
- Full software package (Cross Assembler, debugger)



PDIP28



PSO28



CDIP28

(Ordering Information at the end of the datasheet)

1 GENERAL DESCRIPTION

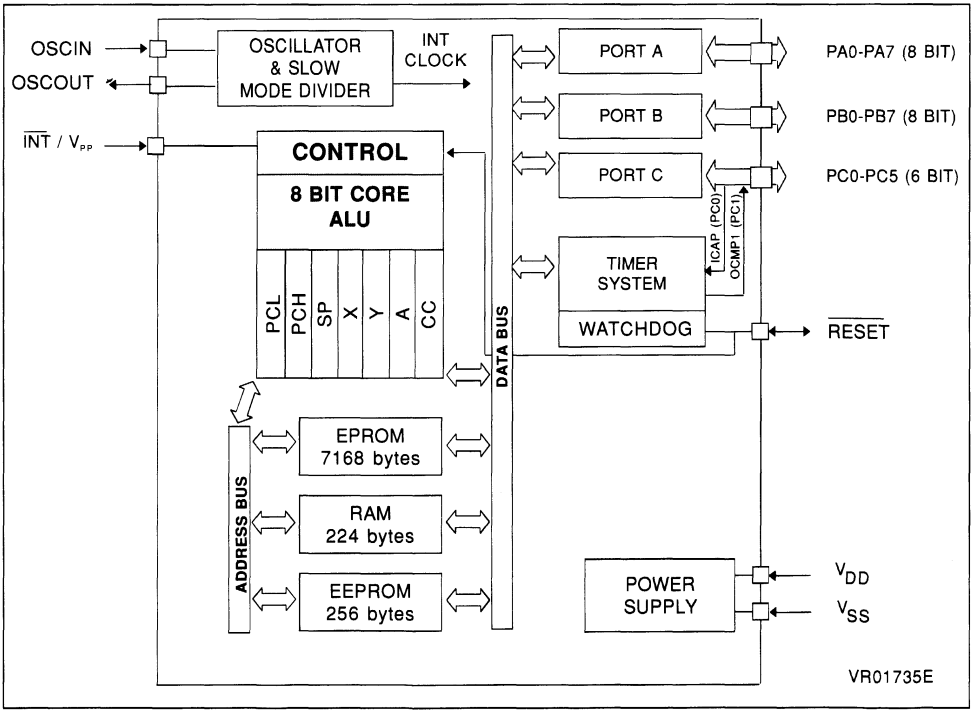
1.1 INTRODUCTION

The ST72E94 and ST72T94 (following mentioned as ST72E94) are EPROM members with EEPROM of the ST72 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developped and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices. **THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST7294 AND ST7293 ROM-BASED DEVICES FOR FURTHER DETAILS.**

The EPROM ST72E94 may be used for the prototyping and the pre-production phases of development, can be configured as either a standalone microcontroller with 7K bytes of on-chip ROM, either as a microcontroller able to manage external memory.

The ST72E94 is a HCMOS microcontroller unit (MCU) from the ST72 family. It is based around an industry standard 8 bit core and offers an enhanced instruction set. The processor runs with an external clock at 4 MHz with a 5V supply and 2MHz with a 3V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST72E94 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST72E94 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes an on-chip oscillator, CPU, EPROM, RAM, EEPROM, I/O, and one timer with 1 input capture and 2 output compare systems.

Figure 1. ST72E94 Block Diagram



1.2 PIN DESCRIPTION

V_{DD}. Single power supply voltage 3 to 5.5V.

V_{SS}. Ground

OSCin, OSCout. Oscillator input and output pins. These pins are to be connected to a parallel resonant crystal or ceramic resonator. An external clock source can also be inputed thru OSCin.

$\overline{RESET}$. The active low input signal forces the initialization of the MCU. This event is the first priority non maskable interrupt. This pin is switched output low when the Watchdog has released. It could be used to reset external peripherals.

$\overline{INT}/V_{PP}$ is the external interrupt signal. Software configuration allows four triggering modes. In the EPROM programming Mode, this pin acts as the programming voltage input V_{PP}.

ICAP (PC0). Input capture signal going to the TIMER system. This signal, according to a mask option, can be an ICAP pin or PC0 pin. When PC0 is defined as ICAP, the internal pull-up resistor is not connected.

OCMP1 (PC1). Output compare signal coming from the TIMER system. This output signal, according to a mask option, can be an OCMP1 pin(for output compare 1 of the timer) or PC1 pin. When PC1 is defined as OCMP1, the internal pull-up resistor is not connected.

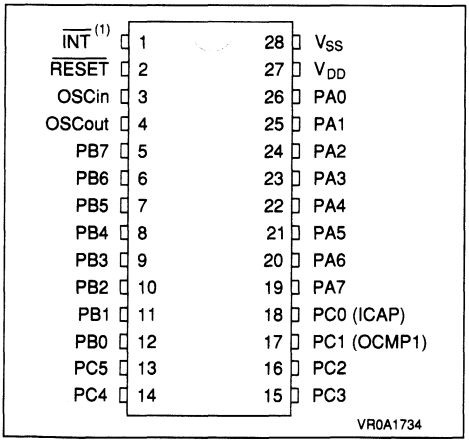
PA0-PA7, PB0-PB7, PC0-PC5. These 22 lines are standard I/O lines, programmable as either input or output.

- PORT A. 8 Standard I/O lines, accessed through DDRA and DRA Registers. According to a bit of the byte option, outputs can be defined as a standard push-pull output port or as an open drain output port. According to a bit of the byte option, a pull-up resistors (250kΩ typical at V_{DD}=3.5V) can be added on each line when it is defined as an input.

- PORT B. 8 Standard I/O lines accessed through DDRB and DRB Registers. According to a bit of the byte option, a pull-up resistor (250kΩ typical at V_{DD}=3.5V) can be added on each line when it is defined as an input.

- PORT C. 6 Standard I/O lines accessed through DDRC and DRC Registers. According to a bit of the byte option, these 6 lines can become 6 falling edge sensitive interrupt lines all linked to a single interrupt vector or 6 standard input ports. When these 6 lines are enabled as inputs, they are tied to V_{DD} through an internal pull-up resistor (250kΩ typical at V_{DD} = 3.5V). These negative edge sensitive interrupt lines can wake-up the ST72E94 from WAIT or HALT mode. This feature allows to build low power applications when the ST72E94 can be waken-up from keyboard push.

Figure 2. Pin Configuration



Note 1. This pin is also the V_{PP} input for EPROM based device

PIN DESCRIPTION (Continued)

Table 1. ST72E94 Pin Configuration

Name	Function	Description	Pin Assignment
$\overline{INT}/V_{PP}$	I	Interrupt / EPROM Programming Voltage	1
$\overline{RESET}$	I/O	Reset	2
OSCin	I	Oscillator	3
OSCout	O	Oscillator	4
PB7	I/O	Standard Port (bit programmable)	5
PB6	I/O	Standard Port (bit programmable)	6
PB5	I/O	Standard Port (bit programmable)	7
PB4	I/O	Standard Port (bit programmable)	8
PB3	I/O	Standard Port (bit programmable)	9
PB2	I/O	Standard Port (bit programmable)	10
PB1	I/O	Standard Port (bit programmable)	11
PB0	I/O	Standard Port (bit programmable)	12
PC5	I/O	Standard Port (falling edge interrupt line)	13
PC4	I/O	Standard Port (falling edge interrupt line)	14
PC3	I/O	Standard Port (falling edge interrupt line)	15
PC2	I/O	Standard Port (falling edge interrupt line)	16
PC1 (OCMP1)	I/O	Standard Port (falling edge interrupt line) or output compare	17
PC0 (ICAP)	I/O	Standard Port (falling edge interrupt line) or input capture	18
PA7	I/O	Standard Port (bit programmable)	19
PA6	I/O	Standard Port (bit programmable)	20
PA5	I/O	Standard Port (bit programmable)	21
PA4	I/O	Standard Port (bit programmable)	22
PA3	I/O	Standard Port (bit programmable)	23
PA2	I/O	Standard Port (bit programmable)	24
PA1	I/O	Standard Port (bit programmable)	25
PA0	I/O	Standard Port (bit programmable)	26
V_{DD}		Power Supply	27
V_{SS}		Ground	28

1.3 CENTRAL PROCESSING UNIT

1.3.1 Introduction

The CPU has a full 8-bit architecture. Six internal registers allow efficient 8-bit data manipulations. The CPU is able to execute 74 basic instructions. It features 10 main addressing modes. It is able to address 8192 bytes of memory and registers with its program counter.

1.3.2 CPU Registers

The 6 CPU registers are shown in the programming model in Figure 3. Following an interrupt, the registers are pushed onto the stack in the order shown in Figure 4. They are popped from stack in the reverse order. The Y register is not affected by these automatic procedures. The interrupt routine must therefore handle it, if needed, through the POP and PUSH instructions.

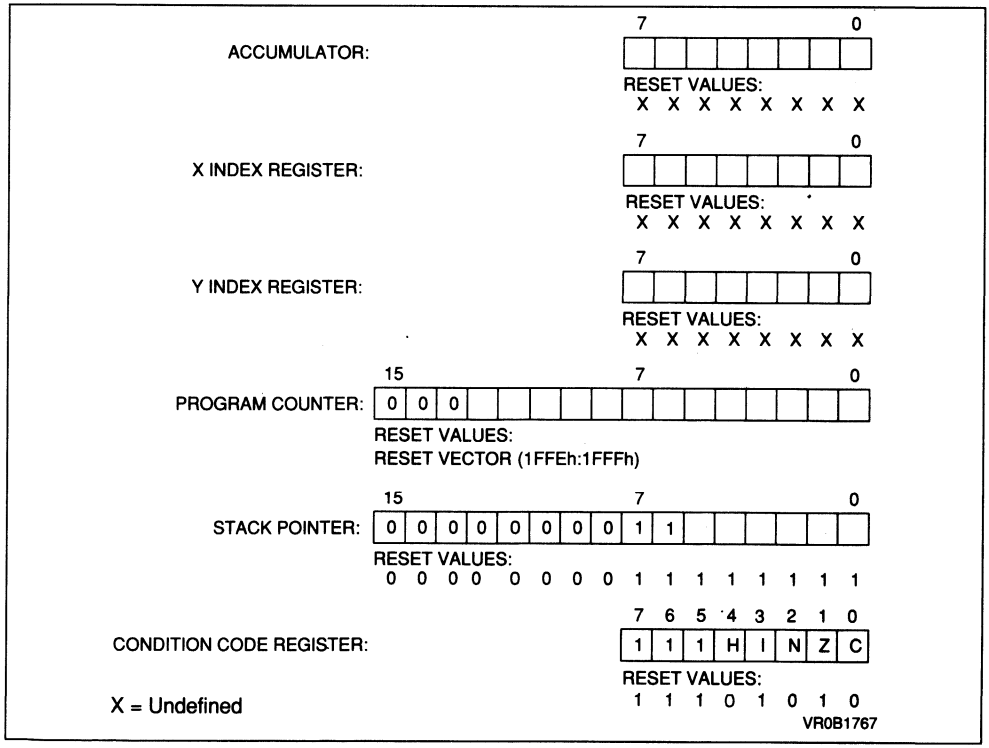
Accumulator (A). The accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations as well as data manipulations.

Index Registers (X and Y). These 8-bit registers are used to create effective addresses or as temporary storage area for data manipulations. The cross assembler generates a PRECEDE instruction (PRE) to indicate that the following instruction refers to the Y register. The Y register is never automatically stacked. Interrupt routines must push or pop it by using the POP and PUSH instructions.

Program Counter (PC). The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. In the ST72E94, only the 13 low order bits are used, bits 13, 14 and 15 are forced to "0".

Stack Pointer (SP). The stack pointer is a 16-bit register. The 6 least significant bits contain the address of the next free location of the stack. The 10 most significant bits are forced as indicated in Figure 3. They are reserved for future extension of ST72 family.

Figure 3. Programming Model



CENTRAL PROCESSING UNIT (Continued)

The stack is used to save the CPU context on subroutines calls or interrupts. The user can also directly use it through the POP and PUSH instructions.

After a MCU reset or after the reset stack pointer instruction (RSP), the stack pointer is set to its upper value (0FFh). It is then decremented after data has been pushed onto the stack and incremented after data is popped from the stack. When the lower limit is exceeded, the stack pointer wraps around to the stack upper limit. The previously stored information is then over written and therefore lost.

A subroutine call occupies two locations and an interrupt five locations.

1.3.3 Condition Code Register (CC).

The condition code register is a 5 bit register which indicates the result of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. The following paragraphs describe each bit.

Half carry bit (H). The H bit is set to 1 when a carry occurs between the bits 3 and 4 of the ALU during an ADD or ACC instruction. The H bit is useful in BCD arithmetic subroutines.

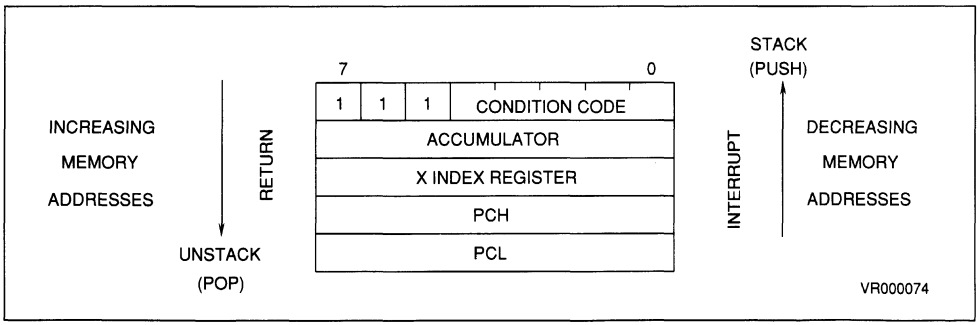
Interrupt mask (I). When the I bit is set to 1, all interrupts are disabled. Clearing this bit enables them. Interrupts requested while I is set are latched and can be processed when I is cleared (only one interrupt request per interrupt enable flag can be latched).

Negative (N). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is negative (i.e. the most significant bit is a logic 1).

Zero (Z). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

Carry/Borrow (C). When set, C indicates that a carry or borrow out of the ALU occurred during the last arithmetic operation. This bit is also affected during bit test, branch, shift and rotate instructions.

Figure 4. Stacking Order



1.4 MEMORY MAP

As shown in Figure 4, the MCU is capable of addressing 8192 bytes of memory and I/O registers. In the ST72E94, 7696 of these bytes are user accessible.

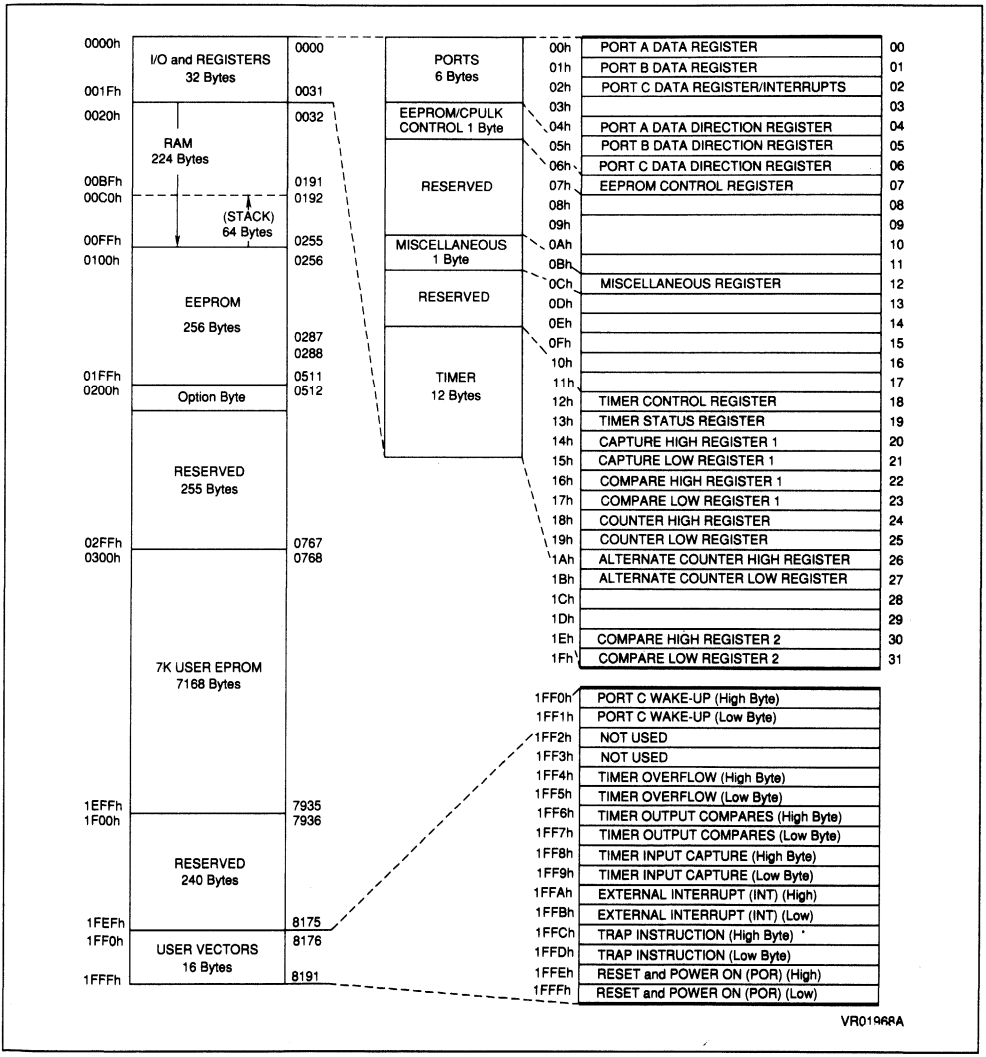
Note:

In the ST7293 only 3.25K bytes are user accessible. This should be taken into account by the user when programming the ST72E94 to emulate the ST7293.

The locations consist of 32 bytes of I/O registers (only 20 are used), 224 bytes of RAM, 256 bytes of EEPROM and 7Kbytes of user ROM. The RAM space includes 64 bytes for the stack from 0FFh to 0C0h. Programs that only use a small part of the allocated stack locations for interrupts and/or subroutine stacking purpose can use the remaining bytes as standard RAM locations.

The highest address bytes contains the user defined reset and interrupt vectors.

Figure 5. Memory Map



1.5 OPTION BYTE

An additional mode is used to configure the part for programming of the EPROM. This is set by a +12.5 voltage applied to the $\overline{INT}/V_{PP}$. The EPROM programming mode is entered during the reset phase if a 12.5 voltage applied to the $\overline{INT}/V_{PP}$ pin with the conditions of pin PC1=1 and pins PC0, PA6 and PA5=0. The 7K byte of EPROM memory may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

The ROM devices of the ST72 family can be configured through mask options. In EPROM devices, most mask options are replaced by EPROM bits grouped in the Option Byte. The configuration of the device is made by programming the Option Byte.

The Option Byte is not in the user memory space. The Option Byte is accessed only if the device is in programming mode and location 0200h is addressed. The EPB provides all the functionality to select and program the Option Byte.

If a device emulated by the ST72E94 does not feature a particular mask option, the corresponding bit is not used. The Timer Clock is defined as $F_{OP}/4$.

7							0
WIW	WDMS	PBIP	PCWS	PC1S	PC0S	PA0S	PAIP

b7 = **WIW:** *Watchdog in Wait.*
1 : Watchdog suspended during Wait
0 : Watchdog active during Wait

b6 = **WDMS:** *Watchdog Mode Select.*
1 : Watchdog in Software Select Mode
0 : Watchdog in auto-enable Mode

b5 = **PBIP:** *Port B Input Pull-up.*
1 : Pull-up enabled or Port B (when Input)
0 : No Pull-up on Port B

b4 = **PCWS:** *Port C Wake-up Select.*
1 : Port C I/O functions enabled
0 : Port C Interrupt Wake-up Inputs enabled

b3 = **PC1S:** *PC1 Select.*
1 : Timer OCMP1 connected to pin 17
0 : PC1 I/O function connected to pin 17

b2 = **PC0S:** *PC0 Select.*
1 : Timer ICAP connected to pin 18
0 : PC0 I/O function connected to pin 18

b1 = **PA0S:** *Port A Output Select.*
1 : Port A Output is Push-pull
0 : Port A Output is Open-drain

b0 = **PAIP:** *Port A Input Pull-up.*
1 : Pull-up enabled on Port A (when Input)
0 : No Pull-up on Port A

1.6 EPROM ERASURE (ST72E94 ONLY)

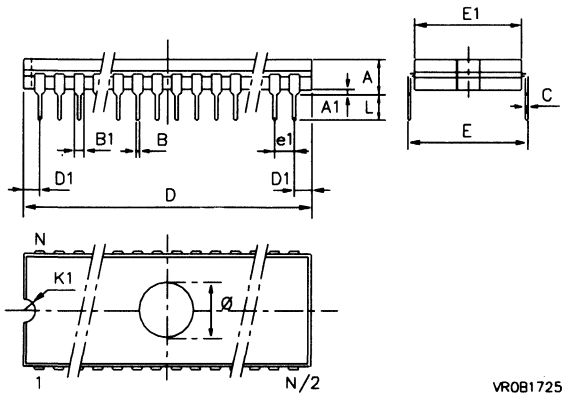
The ST72E94 is erased by exposure to high intensity UV light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current.

It is recommended that the ST72E94 be kept out of direct sunlight because the UV content of sunlight can cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc...) should be placed over the package window if the product is to be operated under these lighting conditions. Covering the window also reduces IDD in stop mode due to photo diode currents.

An Ultraviolet source of wave length 2537Å yielding a total integrated dosage of 15 Watt-sec/cm^2 is required to erase the ST72E94. This device will be erased in 15 to 20 minutes if an UV lamp with a 12mW/cm^2 power rating is placed 1 inch from the lamp without filters.

1.7 PACKAGE MECHANICAL DATA

Figure 6. 28-Ceramic Dual In line Package, 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.17		1.42	.046		.056
C	0.22		0.31	0.009		0.012
D			38.10			1.500
D1	1.52		2.49	.060		.098
E	–	–	–	–	–	–
E1	13.05		13.36	.514		.526
L	3.00			.118		
e1	2.29		2.79	0.090		0.110
Ø	6.86		7.36	.270		.290
	Number of Pins					
N	28					

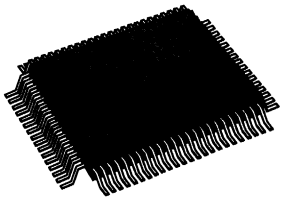
16/32 Bit DSP

STATIC ANSWERING AND RECORDING CHIP

PRELIMINARY DATA

The ST18XSTAR is a high quality low bit rate speech synthesis and recording system. Using ACELP type algorithms for voice compression at 4800bps, it offers the most competitive compromise between speech quality and memory size. It also includes voice synthesis capability, generated from a non volatile memory to produce predefined messages. Including tone and DTMF detectors for remote control operation, it is suitable for use in answering machines, answering telephone sets, cordless answering telephone sets,voice mail systems and memo recorders.

- Low bit rate (4.8kbps) speech coding and decoding system.
- Ultra low bit variable rate (<1.5kbps) speech synthesis message capability.
- Voice storage memory capability up to 32Mbits.
- Integrated implementation on one **D**igital **S**ignal **P**rocessor (DSP) chip.
- Low power design:
  - Single 5V power supply,
  - Maximum active power consumption 500mW,
  - Sleep power Mode 1.5mA for ARAM refresh.
- Reduced size and power consumption suitable for standard voice answering and recording machines, cordless phones with voice recording capability, memo recorders.
- Maximum flexibility provided with emulation ROMless version ST18RXSTAR.
- Extended modes of operations and features :
  - Fast and slow read/skip modes. Messages monitoring.
  - Voice messages for remote operation through telephone line.
  - Possible use of SRAMs, DRAMs, ROMs or EPROMs.
  - Advanced error correction algorithms allowing use of ARAMs.
  - Programmable call progress and call waiting tone generators/detectors including DTMF,comply with PAA/TPA/AGH/1764 specifications.
  - Programmable voice activity detection for silence compression.
  - Programmable output attenuation level (for remote call screening).
  - Wide dynamic range (48dB).
  - PCM 64Kbps coding mode for high-quality incoming/outgoing messages.
- Versatile Interfaces
  - 3 to 1 muxed single-ended A/D input.
  - 2 D/A independently programmable output drivers.
  - On-chip converters.
  - Host processor parallel interface.



PQFP100

(Ordering information at the end of the datasheet)

1PIN DESCRIPTION

1.1 ST18XSTAR PIN DESCRIPTION

Warning: *This data sheet is related to ST18XSTAR. Final pinout and pin number assignement will be described in the next version.*

Storage Memory Interface (30 pins)

Pin Name	Type	Description
MD0-MD7	I/O	Data Bus: 1-bit or 4-bit DRAM's, ARAM's; 8-bit ROM's, EPROM's, SRAM's
MA0-MA10	O	Multiplexed Address pins for A/DRAM's Non Multiplexed Low Address pins for other memories
MA11-MA16	O	Non Multiplexed High Address pins
$\overline{RAS0}$-$\overline{RAS1}$	O	Row Address Select pins for A/DRAM's: Active Low
$\overline{MCS}$	O	Chip Select pin for SRAMS and EPROMS: Active Low
$\overline{CAS}$	O	Column Address Select pin for A/DRAM: Active Low
$\overline{MWE}$	O	Memory Write Enable Active Low

A/D and D/A Converters (13 pins)

Pin Name	Type	Description
VRH		High Reference Voltage
VRL		Low Reference Voltage
VCM		Common Mode Voltage
ADIN0-ADIN2	I	Analog Inputs
DAOUT0-DAOUT1	O	Analog Inputs
AV_{DD}	I	Analog Section Positive Supply
AV_{SS}	GND	Analog Section Ground
ABIAS	I	Analog Section Bias Control

PIN DESCRIPTION (Continued)

Host Interface/Mailbox (13 pins)

Pin Name	Type	Description
SD0-SD7	I/O	System Data Bus used for exchanges between a host and the ST18XSTAR
$\overline{SRD}$	I	Synchronizes the read cycles for the system bus
$\overline{SWR}$	I	Synchronizes the write cycles for the system bus
$\overline{SCS}$	I	Mailbox Chip Select
DTOM	O	Handshake output line with microcontroller
MTOD	I	Handshake input line with microcontroller

Synchronous Double Buffered SSI (4 pins)

Pin Name	Type	Description
FS	I/O	Transmit and Receive Frame synchronous
BCLK	I/O	Transmit and Receive Clock
DX	O	Transmit Data
DR	I	Receive Data

Clocks and Control (13 pins)

Pin Name	Type	Description
$\overline{RESETC}$	I	Reset of the DSP Core: Active Low
$\overline{RESET}$	I	Reset of the DSP and Peripherals: Active Low
XTAL	O	Internal Oscillator Output for Crystal (4.096MHz): No connect if not used
EXTAL	I	External Clock or Internal Oscillator input
$\overline{HALT\text{-}NOP}$	I	Emulation pin: Reserved
$\overline{TEST1}$	I	Reserved
$\overline{TEST2}$	O	Reserved
$\overline{TEST3}$	I	Reserved
$\overline{TEST4}$	O	Reserved
$\overline{TEST5}$	I	Reserved
$\overline{TEST6}$	I	Reserved
$\overline{TEST7}$	O	Reserved
$\overline{TEST8}$	I	Reserved

PIN DESCRIPTION (Continued)

Boundary Scan (11 pins)

A set of 11 signals are dedicated for testing/emulating the ST18XSTAR. These signals are used in a development phase, associated with the SGS-THOMSON ST18932 Boundary Scan development tools, to debug the application hardware and software. If not used the corresponding input signals must be grounded.

Pin Name	Type	Description
SCIN	I	Scan Data Input
SCCLK	I	Scan Clock
SCOUT	O	Scan Data Output
BOS	I	Begin of Scan Control
EOS	I	End of Scan
MC0-MC2	I	Mode Control
SBACK	O	Software Breakpoint Acknowledge
MCI	O	Multicycle Instruction
RDYS	O	Ready to Scan Flag

Digital Power Supply (10 pins)

Pin Name	Type	Description
V_{DD}	I	Positive Supply
V_{SS}	GND	Digital Ground

2 FUNCTIONAL OUTLINE

The ST18XSTAR is a fully integrated implementation of the telephone static answering and recording machine functions. Except for the message storage memory, it comprises all the necessary parts for a full featured answerer.

The ST18XSTAR realizes the following functions under host control:

- 12-bit A/D (Delta-Sigma) and 10-bit D/A conversion.
- storage memory interface, supporting up to two chips 1Mx4, 4Mx1, 4Mx4 DRAM's or ARAM's and ROMs/EPROMs.
- low-bit rate synthesized speech capability.
- 4800 bps voice compression/decompression.
- voice activity detection for silence compression.
- silence play-back with confident noise insertion.
- error correction on mass storage data when ARAM is used.
- DTMF and programmable call progress tone detection.
- one or two frequency and level programmable tones generation with DTMF generation capability.

It does exist in an emulation version with a full access to the DSP program address and instruction bus called ST18RXSTAR for Romless and eXternal host. The standard version incorporates the DSP software in a ROM and is named ST18XSTAR.

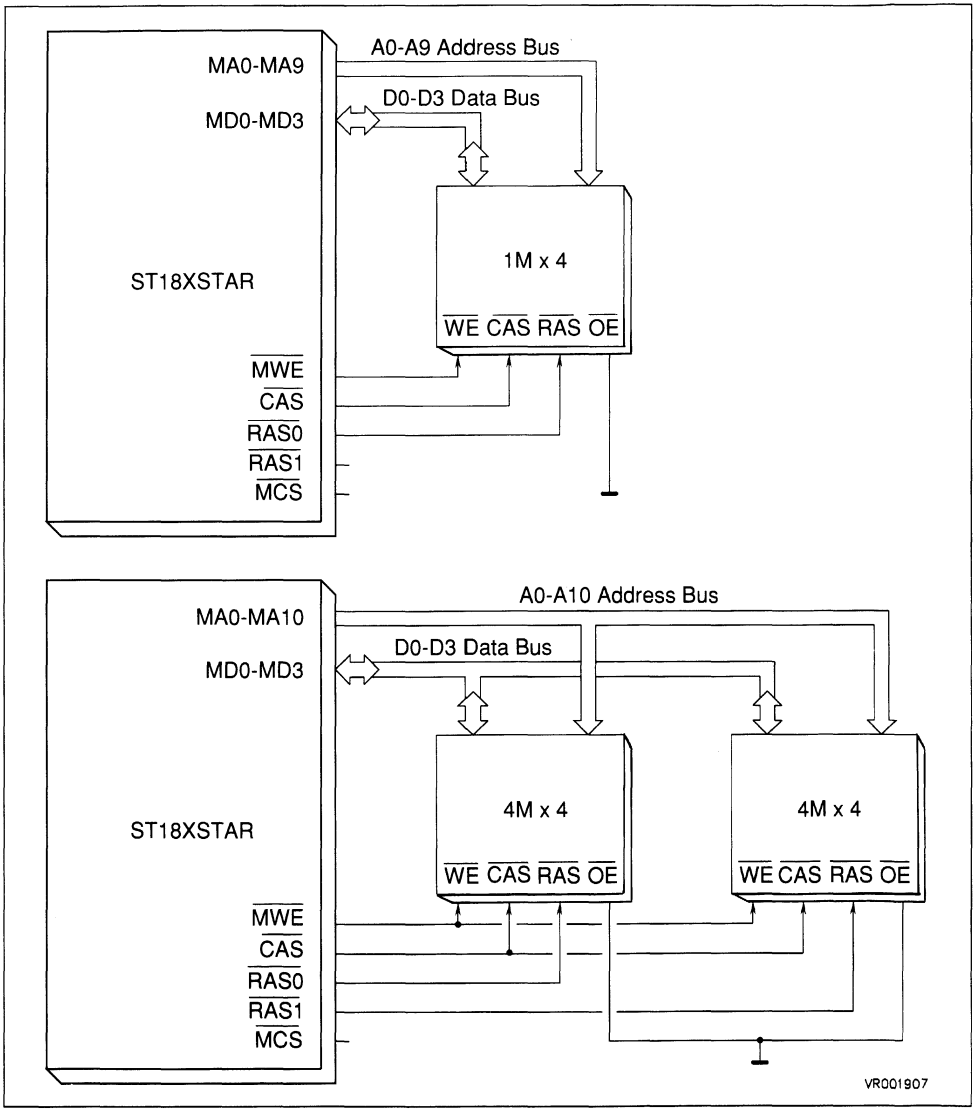
3 INTERFACES

3.1 INTERFACE WITH USER EXTERNAL MEMORIES

For the user messages storage one or two ARAM/DRAM chips can be connected to the ST18XSTAR. Chips of 4Mx1, 1Mx4 and 4Mx4 are accepted. If two chips are used, they must be of the same organisation.

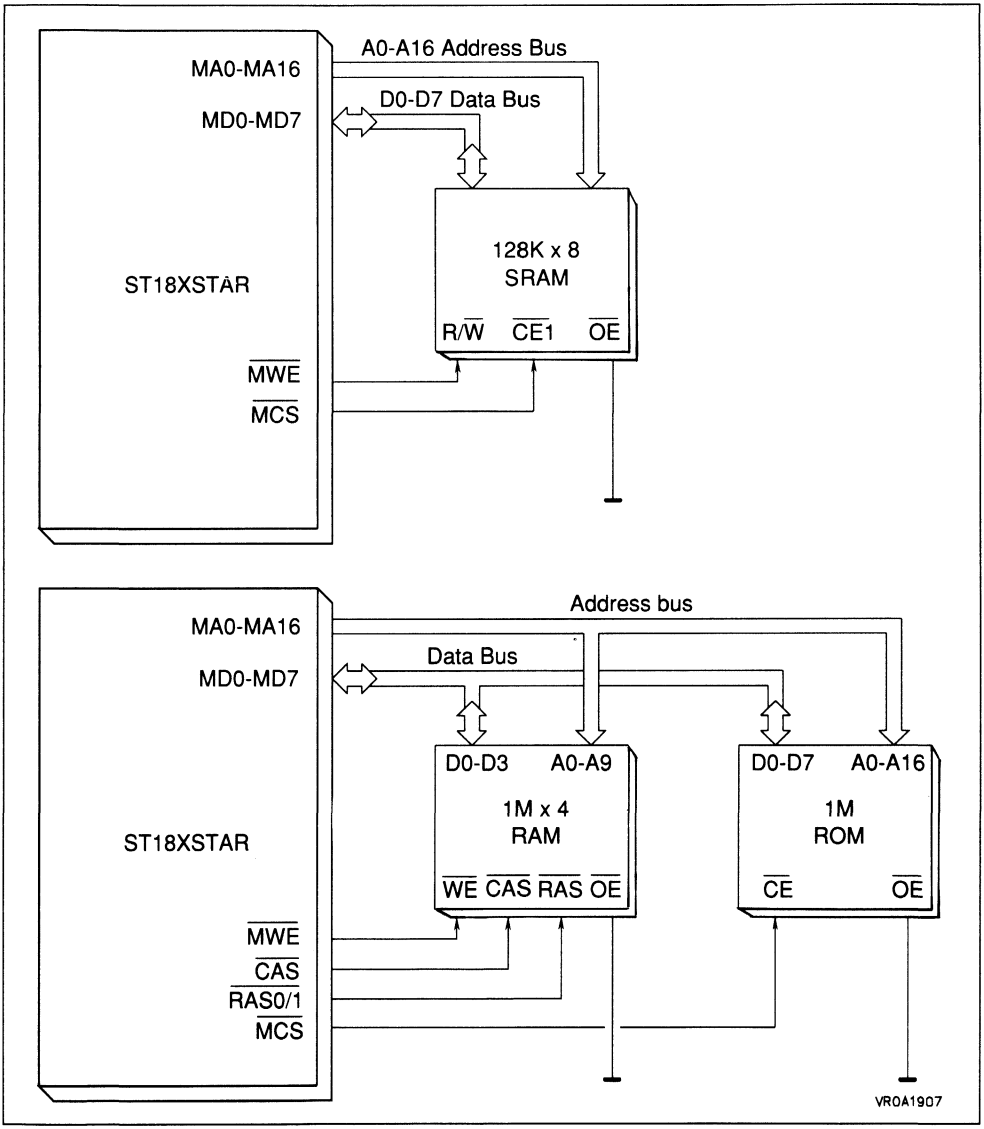
Below are connection examples. Banks of four 1 bit wide chips might of course replace the 4 bit wide chips.

Figure 1. INTERFACE WITH USER EXTERNAL



INTERFACES (Continued)

Figure 2. INTERFACE WITH USER EXTERNAL MEMORIES (Continued)



INTERFACES (Continued)

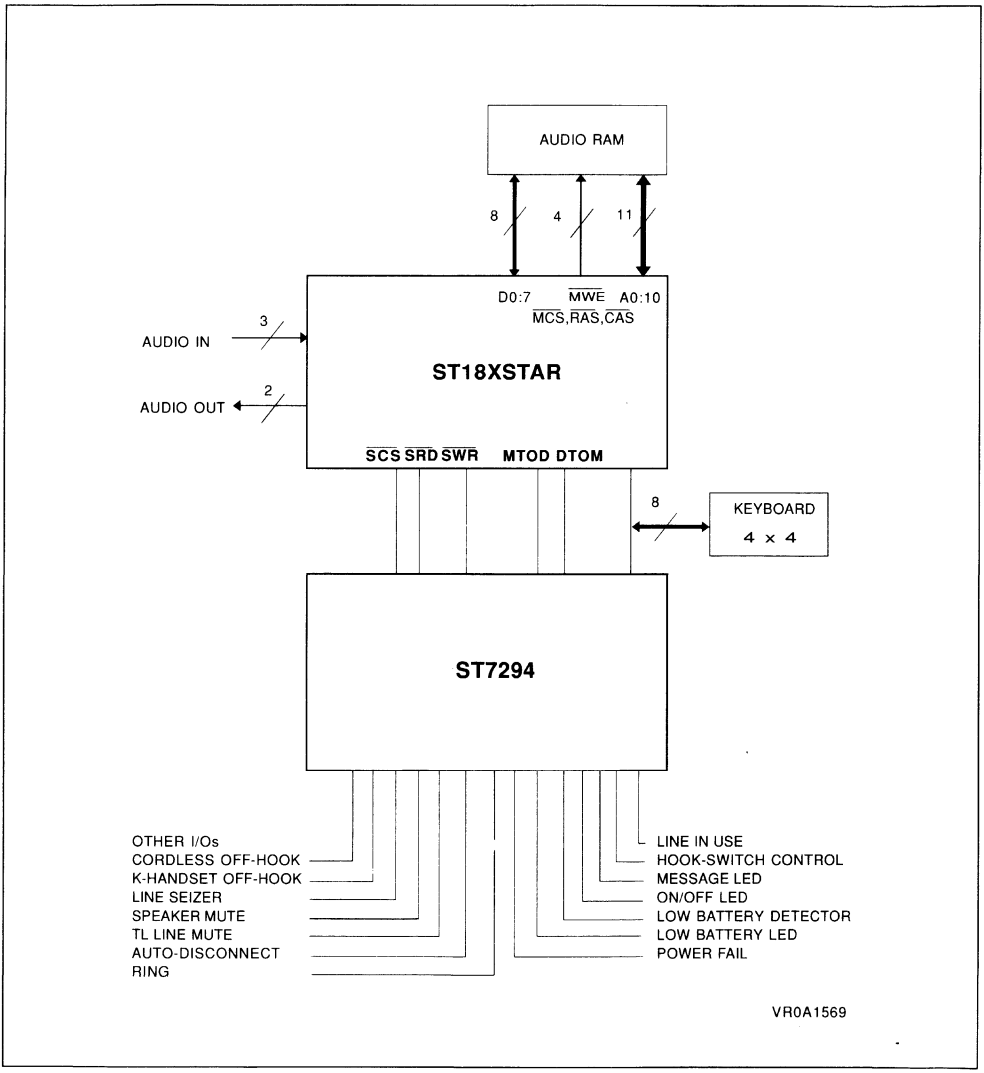
3.2 INTERFACE WITH MANUFACTURER MEMORIES

The manufacturer may create in ROMs, SRAMs or EPROMs predefined messages allowing for example remote control operation, time stamp, etc.. These memories can be connected to the storage memory interface part of the chip thus offering a large flexibility of choices.

3.3 MICROCONTROLLER INTERFACE

The recommended mode of interface between the ST18XSTAR is the host interface mailbox. Figure 3 with a ST7 type microcontroller. However, use with any other micro is possible.

Figure 3. Microcontroller Interface typical application example.



INTERFACES (Continued)

Connection Between ST18XSTAR and MCU

This interface is realized through :

- 8 bi-directional I/O lines (SD0-SD7); these lines can also be shared with an external keyboard.
- 3 control signals : $\overline{SCS}$ (Mailbox Chip Select), $\overline{SRD}$ (Read) and $\overline{SWR}$ (Write).
- 2 synchronization signals : MTOD and DTOM

DSP access sequence:

The data communication between microcontroller and ST18XSTAR is always initiated by the microcontroller and consist generally of a sequence of data exchanges. The $\overline{SRD}$ and $\overline{SWR}$ pins (active low) allow the microcontroller to READ and WRITE respectively the mailbox.

During any data transmission (unique or multiple), a third wire , $\overline{SCS}$ must be maintained to a low level in order to select the ST18XSTAR in the case when the SD0-SD7 lines are also used to scan the keyboard.

Protocol of the data exchange synchronization

Two handshake signals are used to synchronize a bidirectional data exchange between the ST18XSTAR and the microcontroller. Messages may consist of a single or multiple bytes.

MTOD. Signal driven low by the microcontroller to indicate :

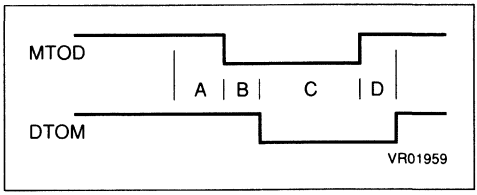
- that a data has been written into the ST18XSTAR mailbox (RIN register).
- or that the micocontroller is ready to read a new byte in the mailbox (ROUT register).

DTOM. Signal generated by the ST18XSTAR and may be connected to an interrupt input of the microcontroller, indicate to the microcontroller that a byte is available in the mailbox (ROUT register) and can be read by the microcontroller.

A communication between the microcontroller and the ST18XSTAR generally consists of a sequence of data exchanges and is always initiated by the microcontroller. For example, the micrcontroller can load a "DTMF request" and get back six bytes of information on DTMF status.

Due to real-time processing constraints, the ST18XSTAR generally reserves a time slot for communication with its microcontroller at the end of each 30 ms speech frame.The SYNCHRO request (See commands description) can be used by the microcontroller to get synchronized with the ST18XSTAR communication window.

Figure 4. Communication Handshake Protocol



Step A:

(MCU steps) may exist or not if no relevant data to write into RIN (when it requests a sequence of status bytes the MTOD line is asserted low directly).

Both MTOD and DTOM lines are high (idle mode).

The microcontroller write a command
or The microcontroller write an operand of command into the mailbox(RIN)

then brings the MTOD signal low.

Step B:

The ST18XSTAR

Read command in RIN, decode, process, and write data or status in ROUT
or Read operand in RIN
or Write status byte into ROUT

then brings the DTOM signal low.

Step C:

The microcontroller read data if there is a significant data in the mailbox (ROUT)

then brings the DTOM signal high.

Step D (ST18XSTAR step):

After MTOD rising edge, the DTOM signal goes high.

Step E: handshake idle state

This sequence of steps A-B-C-D-E can be repeated several times : when a command or request involves several operands to be sent by the microcontroller, or when a command or request from the microcontroller requires several status or parameter bytes to be return by the ST18XSTAR.

INTERFACES (Continued)

3.4 ANALOG INTERFACE

Three single-ended analog inputs are provided. The ST18XSTAR contains a register that allows to select one input among the three.The maximum input swing is 2.5V peak-peak. The input impedance is essentially capacitive. Its value is less than 20pF. Resolution of the A/D is 12 bits.

Two analog outputs are provided. Each one can be put in active state or driven to VCM state. The output swing is 280mV peak-peak on a 1kΩ load. Resolution of the D/A is 10 bits. The maximum current of the output buffer is 200µA. A 16-level attenuation is provided, from 0 to -28dB (+ infinite attenuation level, driven to VCM state) by 2dB steps.

4 STORAGE MEMORY MANAGEMENT

4.1 STORAGE POLICY

The ST18XSTAR partitions memory into sectors, and freely allocates sectors to messages through pointers. The sector size and the number of addressable sectors are dependant upon the type of memory chips.

Table 1. Types of Memory Chips

Type of Memory	Sector size	Number of Sectors
4M x 4bit	128K	256
4M x 4bit	32K	256
1M x 4bit	32k	256
1M x 1bit	32K	64

4.2 INCOMING MESSAGES ALLOCATION TABLE DESCRIPTION

The allocation table is a 512x16 bit word table allowing up to 128 messages depending on the message lengths.

5 SOFTWARE MANAGEMENT OF ST18XSTAR

5.1 COMMAND AND REPORT DESCRIPTION

Introduction

The ST18XSTAR operation is fully controlled by the host microcontroller. It receives command bytes and returns report bytes.

The command may indicate :

- a mode, i.e. the background task executed by the ST18XSTAR.
- a request which will be executed during the next communication window.

The status byte indicates the current operating mode, the occurence of an event (end of message, storage memory full,...) or an error (invalid command,...).

Communication description

The microcontroller sends to the ST18XSTAR a command, which consists of one opcode byte, followed by zero, one or more operands. The ST18XSTAR returns to the microcontroller a report which consists of one status byte, followed by zero, one or more operands.

Figure 5. Opcode Byte

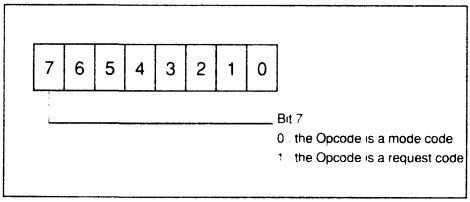
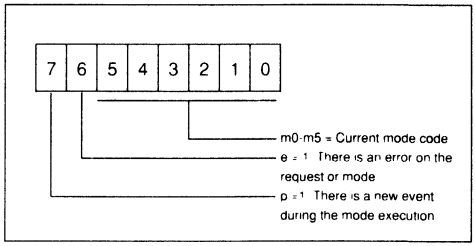


Figure 7. Status Byte

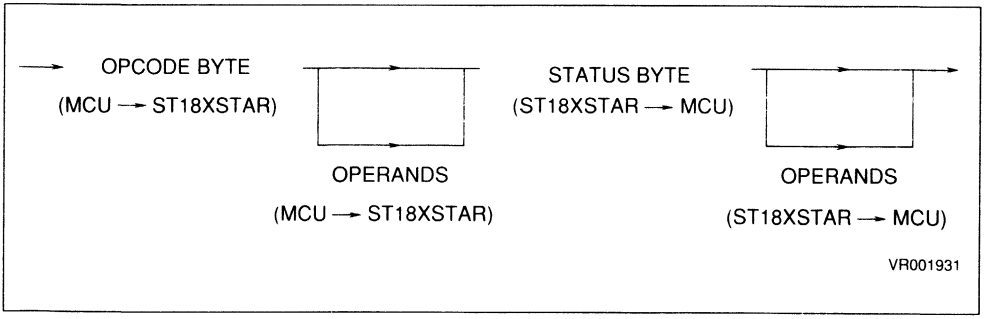


Current mode code :

WAIT mode set

IDLE	= 000001
DTMF	= 000010
DEFAULT	= 000011
TONE DETECTION	= 001000
TONE GENERATION	= 001100
RECORD	= 010000
PLAY-BACK	= 010001
SPEECH SYNTHESIS	= 010010

Figure 6. Communication Description



SOFTWARE MANAGEMENT OF ST18XSTAR (Continued)

Modes description

When the microcontroller sends a mode command, the ST18XSTAR returns a status byte and changes the background task.

"WAIT" mode set

The WAIT mode set contains three differents modes : IDLE, DTMF, and DEFAULT. In this mode, no speech processing task is performed.

"IDLE"

In this mode, the ST18XSTAR polls microcontroller commands, without performing any task.

COMMAND FORMAT:
byte 1 = 00000100

REPORT FORMAT:
byte 1 = status byte

"DTMF"

The "DTMF" performs the DTMF and energy detection. This mode operates properly only if "DTMF" initialisation has been made before the mode call.

COMMAND FORMAT :
byte 1 = 00001000

REPORT FORMAT :
byte 1 = status byte

"DEFAULT"

The "DEFAULT" mode performs the mode selected with the "DEFAULT" initialisation request, in practice "IDLE" or ""DTMF". If no initialisation is made, the default mode is "IDLE".

COMMAND FORMAT :
byte 1 = 00001100

REPORT FORMAT :
byte 1 = status byte

"TONE GENERATION"

"TONES GENERATION" performs the generation of one or two tones. This mode operates properly only if "TONE GENERATION" initialisation has been processed before the mode call. The tone frequency and amplitude values are provided by the microcontroller during the "TONE GENERATION" initialisation request.

COMMAND FORMAT :
byte 1 = 00100000

REPORT FORMAT:
byte 1 = status byte

"TONE DETECTION"

"TONE DETECTION" performs the detection of one or two tones. This mode works properly only if "TONE DETECTION" initialisation has been processed before the mode call. The filter coefficients are defined during the "TONE DETECTION" initialisation request.

COMMAND FORMAT:
byte 1 = 00011000

REPORT FORMAT:
byte 1 = status byte

"RECORD"

In this mode, the ST18XSTAR performs speech compression and records messages into the ARAM. This mode operates properly only if "RECORD" initialisation has been processed before the mode call. While in this mode, the ST18XSTAR automatically performs DTMF and energy detection.

COMMAND FORMAT :
byte 1 = 01111111
byte 2 = 00000000
byte 3 = nbfr MSB
byte 4 = nbfr LSB

nbfr : number of 30ms speech frames to be processed:

nbfr = 0 mode changing is forced by the microcontroller

nbfr > 0 after nbfr frames processing, the ST18XSTAR automatically enters in the "DEFAULT" mode.

REPORT FORMAT :
byte 1 = status byte

SOFTWARE MANAGEMENT OF ST18XSTAR (Continued)

"PLAYBACK"

In this mode, the ST18XSTAR performs playback of compressed messages stored in the ARAM. This mode operates properly only if "PLAY-BACK" initialisation has been processed before the mode call. While in this mode, the ST18XSTAR automatically performs DTMF and energy detection.

COMMAND FORMAT :
byte 1 = 01111111
byte 2 = 00000001
byte 3 = nbfr MSB
byte 4 = nbfr LSB

nbfr : number of speech frames to be processed :

nbfr = 0 mode changing is forced by the microcontroller

nbfr 0 after nbfr frames processing, the ST18XSTAR automatically enters in the "DEFAULT" mode.

REPORT FORMAT :
byte 1 = status byte

"SPEECH SYNTHESIS"

In this mode, the ST18XSTAR performs speech synthesis word templates stored in a ROM. This mode operates properly only if "SYNTHESIS" initialisation has been processed before the mode call. The message is selected during the "SYNTHESIS" initialisation request. While in this mode, the ST18XSTAR automatically performs DTMF and energy detection.

COMMAND FORMAT :
byte 1 = 01111111
byte 2 = 00000010
byte 3 = nbfr MSB
byte 4 = nbfr LSB

nbfr : number of speech frames to be processed

nbfr = 0 mode changing is forced by the microcontroller

nbfr 0 after nbfr frames processing, the ST18XSTAR automatically enters in the "DEFAULT" mode.

REPORT FORMAT :
byte 1 = status byte

Request description

Status request

"NOP"

This request is allowed with any mode. It can be used to get the status byte value (cf. Introduction).

REQUEST FORMAT :
byte 1 = 10010001

REPORT FORMAT :
byte 1 = status byte

"SYNCHRO"

This request is available with any mode. It allows the communication with the microcontroller to be synchronized with the DSP operation, in order to exchange data every speech frame (typically every 30 ms).

If a SYNCHRO request is sent by the microcontroller during the current frame, it will be answered at the beginning of the communication window allowed by the ST18XSTAR in the next frame.

REQUEST FORMAT :
byte 1 = 10010010

REPORT FORMAT :
byte 1 = status byte

"GET INFORMATION ON EVENT"

This request is available with any mode.
The first byte is the current information status: the error status is cleared at each request execution, the event status is cleared at the beginning of each frame.

The second byte is a memorized information status, which contains the latest no-null error status, and the latest no-null event status. They are cleared when the "GET INFORMATION ON EVENT" request is called.

SOFTWARE MANAGEMENT OF ST18XSTAR (Continued)

INFORMATION BYTE DESCRIPTION :

information byte = wdiomnbe

w = 1 wrong request operand	||	
d = 1 illegal request	||	error
u = 1 user error	||	status
o = 1 overrun	||	
m= 1 memory shortage	||	event
n = 1 nbfr frames processed	||	status
b = 1 message begin reached	||	
e = 1 message end reached	||	

REQUEST FORMAT :
byte 1 = 10010011

REPORT FORMAT :
byte 1 = status byte
byte 2 = dwuomnbe current information byte
byte 3 = dwuomnbe memorized information byte
byte 4 = uuuuuuu if u=1 user error number

Initialisation requests

"AUDIO-RAM INITIALISATION"

This request is only allowed in "WAIT" mode, to define the message storage memory configuration actually used with the ST18XSTAR.
The microcontroller can reserve one part of the audio-RAM memory for its own use.
The message allocation table is re-initialized when this request is executed.

REQUEST FORMAT :
byte 1 = 10100001
byte 2 = 00000000
byte 3 = 000sbmac with
s = 0 dynamic memory (SMI interface)
s = 1 static memory (SMI interface)
b = 0 1 bit word size
b = 1 4 bits word size
m= 0 1 Mw memory size
m= 1 4 Mw memory size
a = 0 dynamic RAM
a = 1 audio RAM
c = 0 1 dynamic memory chip
c = 1 2 dynamic memory chips
byte 4 = rrrrrrrr number of kilobytes reserved for the microcontroller

REPORT FORMAT :
byte 1 = status byte

"CONVERTER INITIALISATION (A/D AND D/A)"

This request in only authorized in a "WAIT" mode.

REQUEST FORMAT :
byte 1 = 10100010
byte 2 = 000000ii input selection :
ii = 00 ADIN0
ii = 01 ADIN1
ii = 10 ADIN2
ii = 11 ADIN2
byte 3 = s00aaaaa initialization of the DAOUT0 output :
s = 1 DAOUT0 is selected
attenuation value on DAOUT0 :
aaaaa = 00000 no attenuation
aaaaa = 00001 1 dB of attenuation
.....
.....
.....
aaaaa = 11100 28 dB of attenuation
aaaaa = 11101 29 dB of attenuation
aaaaa = 11110 infinite attenuation
aaaaa = 11111 infinite attenuation
byte 4 = s000aaa0 initialization of the DAOUT1 output :
s = 1 DAOUT1 is selected
attenuation value on DAOUT1 :
aaaa = 0000 no attenuation
aaaa = 0001 2 dB of attenuation
....
....
....
aaaa = 1110 28 dB of attenuation
aaaa = 1111 infinite attenuation

REPORT FORMAT :
byte 1 = status byte

"AUTOTEST"

This request is only authorized in a "WAIT" mode.

REQUEST FORMAT :
byte 1 = 10100011

REPORT FORMAT :
byte 1 = status byte

SOFTWARE MANAGEMENT OF ST18XSTAR (Continued)

"LOW-POWER STATE"

This request is only authorized in a "WAIT" mode to put the ST18XSTAR in a "low-power" state.
The ST18XSTAR exits from the low-power state as soon as the the microcontroller sends a new command.

REQUEST FORMAT :
byte 1 = 10100100

REPORT FORMAT :
byte 1 = status byte

Mode Initialisation

"IDLE INITIALISATION"

This request is only authorized in a "WAIT" mode.

COMMAND FORMAT :
Mbyte 1 = 10110001

REPORT FORMAT :
byte 1 = status byte

"DTMF INITIALISATION"

This request is only authorized in a "WAIT" mode.

COMMAND FORMAT :
byte 1 = 10110010

REPORT FORMAT :
byte 1 = status byte

"DEFAULT INITIALISATION"

This request is only authorized in a "WAIT" mode.

This request selects the mode processed by a "DEFAULT" mode call.

COMMAND FORMAT :
byte 1 = 10110011
byte 2 = default mode opcode

REPORT FORMAT :
byte 1 = status byte

"TONE GENERATION INITIALISATION"

This request is only authorized in a "WAIT" mode. It defines the frequency and amplitude values of the tones to be generated by the ST18XSTAR.

COMMAND FORMAT :
byte 1 = 10111000
byte 2 = tone frequency 1 MSB
byte 3 = tone frequency 1 LSB
byte 4 = tone amplitude
byte 5 = tone frequency 2 MSB
byte 6 = tone frequency 2 LSB
byte 7 = tone amplitude

REPORT FORMAT :
byte 1 = status byte

"TONE DETECTION INITIALISATION"

This request is only authorized in a "WAIT"mode. It defines the characteristics of the tones to be detected by the ST18XSTAR for line monitoring.

COMMAND FORMAT :
byte 1 = 10111110
byte 2 = to be defined

REPORT FORMAT :
byte 1 = status byte

"RECORD INITIALISATION"

This request is only authorized in a "WAIT" mode. This request creates an entry in the allocations table, and initializes the speech coding.

COMMAND FORMAT :
byte 1 = 10000000
byte 2 = 00000000
byte 3 = 000000FV

F = 0 Error correction disabled
F = 1 Error correction enabled
V = 0 VAD disabled
V = 1 VAD enabled

REPORT FORMAT :
byte 1 = status byte

"PLAYBACK INITIALISATION"

This request is only authorized in a "WAIT" mode.

This request is looking for the entry of the message to be played back.

SOFTWARE MANAGEMENT OF ST18XSTAR (Continued)

COMMAND FORMAT :
byte 1 = 10000000
byte 2 = 00000010
byte 3 = 000000F0
F = 0 Error correction disabled
F = 1 Error correction enabled

REPORT FORMAT :
byte 1 = status byte

"PLAYBACK SPEED INITIALISATION"

This request is only authorized in "WAIT" or "PLAY-BACK" mode. This request selects the play-back speed.

COMMAND FORMAT :
byte 1 = 10000000
byte 2 = 00000011
byte 3 = 000000ss
ss speed
ss = 00 normal speed
ss = 01 low speed (0.7 x normal)
ss = 10 fast speed (1.5 x normal)

REPORT FORMAT :
byte 1 = status byte

"SYNTHESIS INITIALISATION"

This request is only authorized in a "WAIT" mode. It is used to initialize the Speech Synthesis mode.

COMMAND FORMAT :
byte 1 = 10000000
byte 2 = 00000100

REPORT FORMAT :
byte 1 = status byte

Message requests

"MESSAGE RENUMBERING"

This request is authorized only in "WAIT" mode. The ST18XSTAR will renumber all the messages stored in the ARAM, starting from number 1 and incrementing the numbers (with a step 1) in respecting the message order.

REQUEST FORMAT :
byte 1 = 11000001

REPORT FORMAT :
byte 1 = status byte

"CREATE A MESSAGE"

This request is only authorized in "WAIT" mode. The ST18XSTAR will create a new entry in the allocation table.

REQUEST FORMAT :
byte 1 = 11000010
byte 3 = nnnnnnnn message number
byte 4 = 00000ddd day
byte 5 = 000hhhhh hour
byte 6 = 00mmmmmm minute

REPORT FORMAT :
byte 1 = status byte

"DELETE A MESSAGE"

This request is only authorized in "WAIT" mode. The ST18XSTAR will delete the specified message. The number of the remaining messages is not changed.

REQUEST FORMAT :
byte 1 = 11000011
byte 2 = 00nnnnnn message number

REPORT FORMAT :
byte 1 = status byte

"SET CURRENT MESSAGE NUMBER"

This request, only authorized in a "WAIT" mode, selects the number of the message to be played back.

REQUEST FORMAT :
byte 1 = 11000100
byte 2 = 00nnnnnn message number

REPORT FORMAT :
byte 1 = status byte

"MESSAGE SUMMARY"

This request is only authorized in a "WAIT" mode. The ST18XSTAR returns to the microcontroller information on the message memory and allocation table : number of recorded messages, memory and allocation table used.

REQUEST FORMAT :
byte 1 = 11000101

SOFTWARE MANAGEMENT OF ST18XSTAR (Continued)

REPORT FORMAT :
byte 1 = status byte
byte 2 = Number of recorded messages
byte 3 = mmmmmmmm ARAM space used in sectors ($FF = full)
byte 4 = aaaaaaaa Alloc table space used in % ($FF = full)

"INFORMATION ON A SPECIFIED MESSAGE"

This request is only authorized in "WAIT" mode.
The ST18XSTAR returns information on a specified message.

REQUEST FORMAT :
byte 1 = 11000110
byte 2 = nnnnnnnn message number

REPORT FORMAT :
byte 1 = status byte
byte 2 = 00000ddd day
byte 3 = 000hhhhh hour
byte 4 = 00mmmmmm minutes
byte 5 = llllllll message length
byte 6 = llllllll message length

"MESSAGE REWIND"

This request is only authorized in "WAIT" mode.
The ST18XSTAR rewinds backward or skips forward inside the current message.
After rewind, the end of the message can be deleted.

REQUEST FORMAT :
byte 1 = 11000111
byte 2 = 000000rc
rc = 00 rewind and delete until end of message
rc = 01 no action
rc = 10 rewind
rc = 11 skip forward
byte 3 = sqqqqqqq
s = 1 and r = 11 go to end of message
s = 1 and rc = 10 go to beginning of message
byte 4 = pppppppp
When s = 0, the number of frames to re wind or skip is given by qqqqqqqq (MSB) and pppppppp (LSB).

REPORT FORMAT :
byte 1 = status byte

"FIXED MESSAGE COMPOSITION"

This request is only authorized in "WAIT" mode.
The ST18XSTAR specifies the sequence of fixed words to be synthesized.

REQUEST FORMAT :
byte 1 = 11001000
byte 2 = 0000nnnn Number of words to be synthesized
byte k = j 3 <= k <= nnnn+2 The (k-2)th word in the sequence is the word "j" of the phrase.

REPORT FORMAT :
byte 1 = status byte

Detection Requests

"SIGNAL INFORMATION REQUESTS"

Read current energy detection thresholds
This request is available with any mode.

REQUEST FORMAT :
byte 1 = 11010000

REPORT FORMAT :
byte 1 = status byte
byte 2 = 0ddddddd Energy detection threshold (in dB)
byte 3 = 0mmmmmmm Energy missing threshold (in dB)
byte 4 = 0ddddddd 300-550 Hz detection threshold (in dB)
byte 5 = 0mmmmmmm 300-550 Hz missing threshold (in dB)

"PROGRAM CURRENT ENERGY DETECTION THRESHOLDS"

This request is available with any mode.

REQUEST FORMAT :
byte 1 = 11010001
byte 2 = 0ddddddd Energy detection threshold (in dB)
byte 3 = 0mmmmmmm Energy missing threshold (in dB)
byte 4 = 0ddddddd 300-550 Hz detection threshold (in dB)
byte 5 = 0mmmmmmm 300-550 Hz missing threshold (in dB)

REPORT FORMAT :
byte 1 = status byte

SOFTWARE MANAGEMENT OF ST18XSTAR (Continued)

"INFORMATION ON ENERGY LEVEL"

This request is available with any mode.
The ST18XSTAR returns two bytes to give the energy of the received signal.

REQUEST FORMAT :
byte 1 = 11010010

REPORT FORMAT :
byte 1 = status byte
byte 2 = 0ddddddd energy level (in dB)
byte 3 = 0mmmmmmm 300-550Hz signal energy (in dB)

"INFORMATION ON DTMF DETECTION AND ENERGY"

This request is available with any mode.
The ST18XSTAR provides one byte of information on DTMF and energy detection for each 5ms subframe.
For each frame, the ST18XSTAR returns six bytes to give the state of the received signal. For each 5 ms subframe, the state of the signals e, k and v, is as follows :

- E (bit 6) = 1 if energy level of the received signal is higher than the upper threshold
- e (bit 5) = 1 if the 300-550Hz signal is higher than the programmed detection threshold.
- k (bit 4) = 1 if a DTMF value has been decoded
- v (bits 3 to 0) is the DTMF decoded key. This key is valid if k = 1.

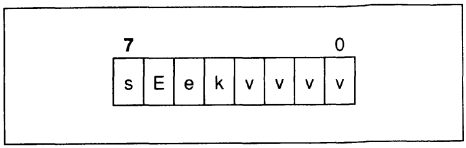
Note :

Only bytes with bit 7 (s) set to "1" are significant, i.e. some bytes are not valid for frame duration shorter than 30ms.

REQUEST FORMAT :
byte 1 = 11010011

REPORT FORMAT :
byte 1 = status byte
byte 2 to byte 7 respectively provide the information for the six 5ms subframes.
Each of these bytes is coded as follows

Figure 8. DTMF Register



"INFORMATION ON TONE DETECTION"

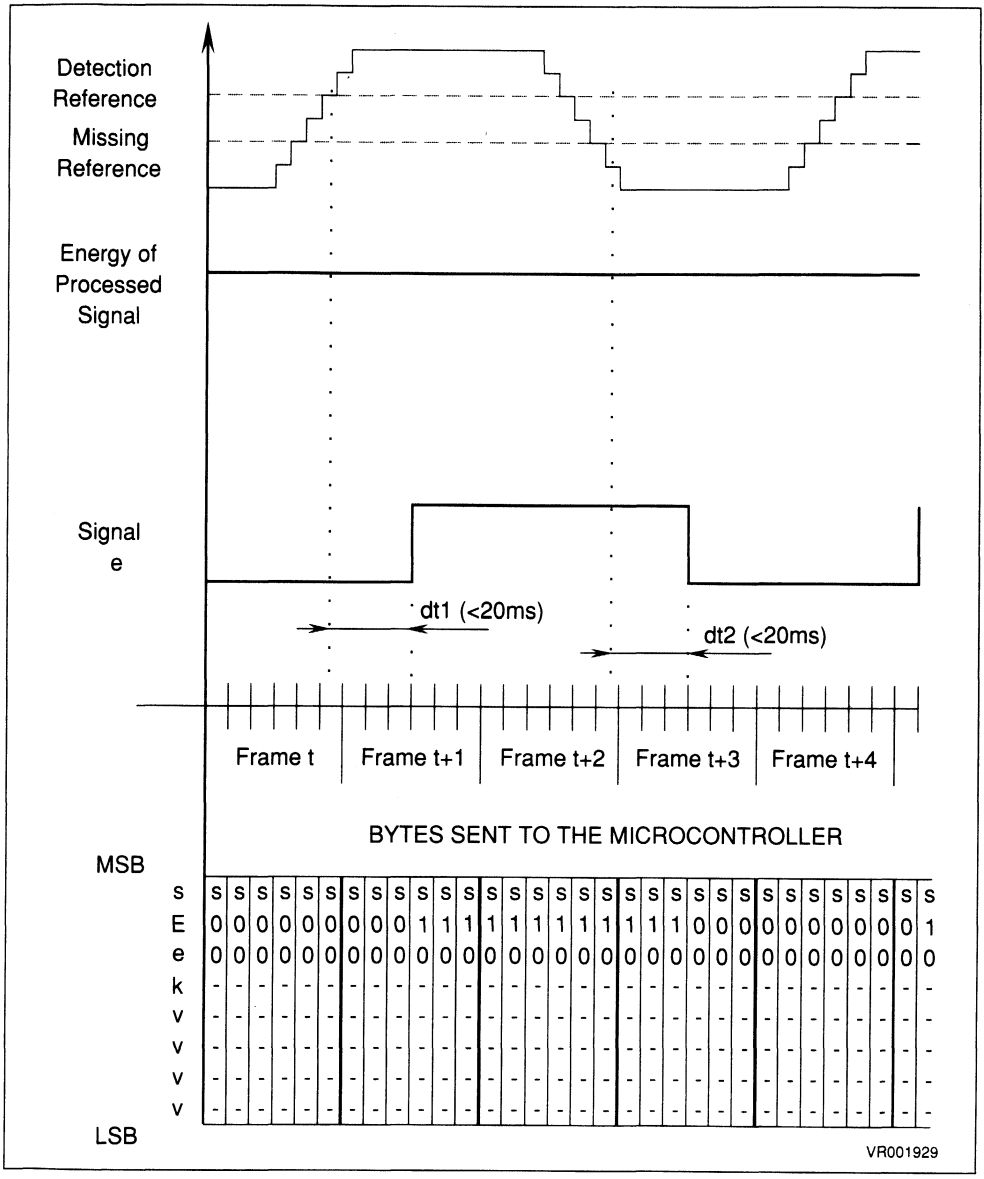
This request is valid only during "TONE DETECTION" mode.
The ST18XSTAR returns one information byte for each 5ms subframe, i.e. for each 30ms frame.

REQUEST FORMAT :
byte 1 = 11010100

REPORT FORMAT :
byte 1 = status byte
byte 2 to byte 7 respectively provide the information for the six 5 ms subframes.
Each of these bytes is coded as follows : each bit corresponds to the result of a filter

SOFTWARE MANAGEMENT OF ST18XSTAR (Continued)

Figure 9. Example of Energy Detection

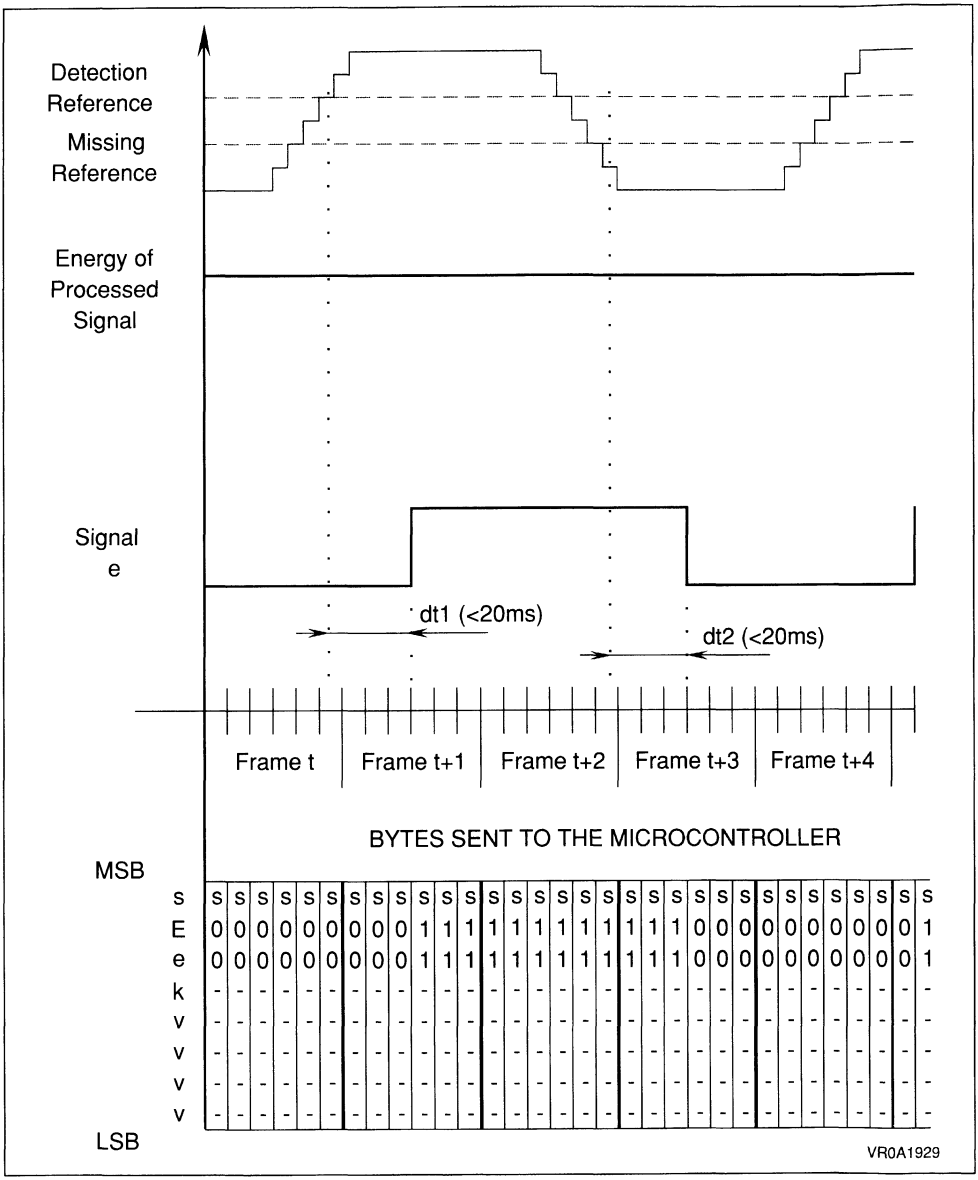


Important note :

With respect to the signal received at the A/D converter input, the information provided by the ST18XSTAR is delayed by a processing time of 30 ms plus the transit time in the digital filters.

SOFTWARE MANAGEMENT OF ST18XSTAR (Continued)

Figure 10. Example of 300-550Hz Energy Detection

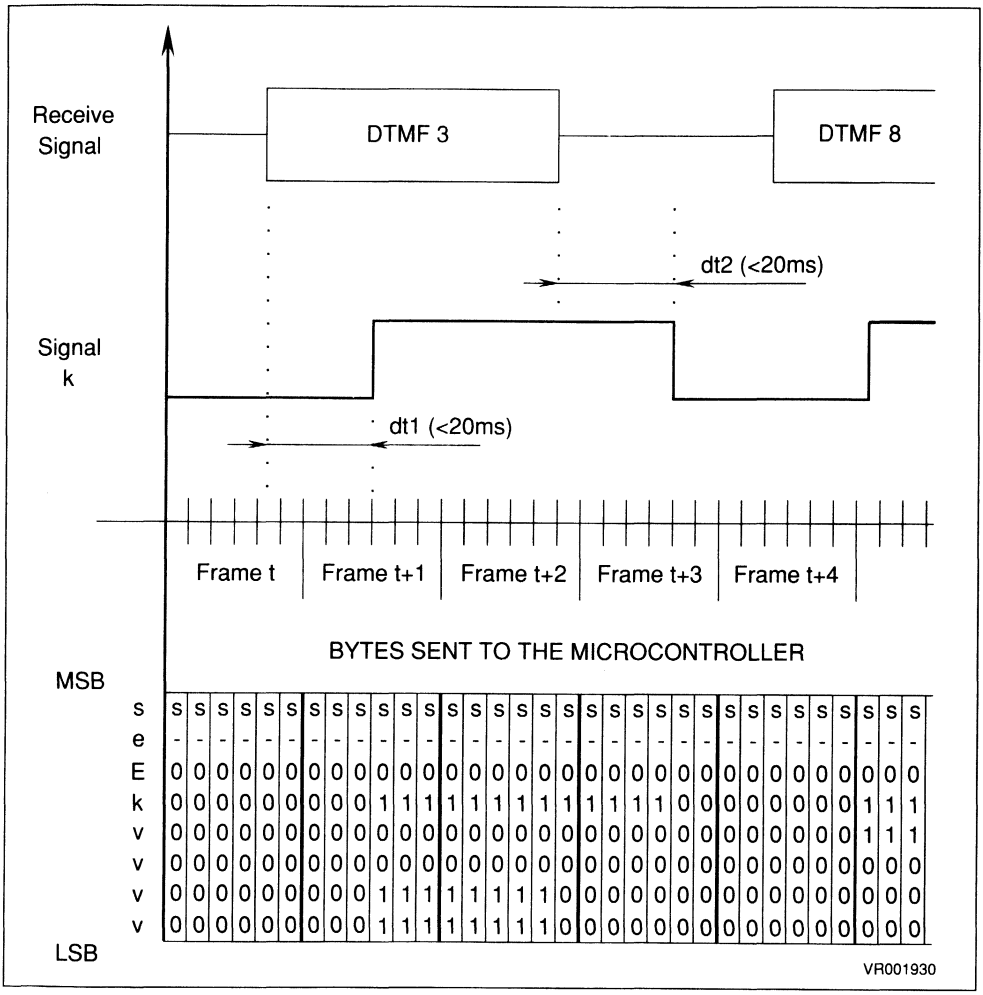


Important note :

With respect to the signal received at the A/D converter input, the information provided by the ST18XSTAR is delayed by a processing time of 30 ms plus the transit time in the digital filters.

SOFTWARE MANAGEMENT OF ST18XSTAR (Continued)

Figure 11. Example of DTMF Detection (Reception of values 3 and 8)



Important note :

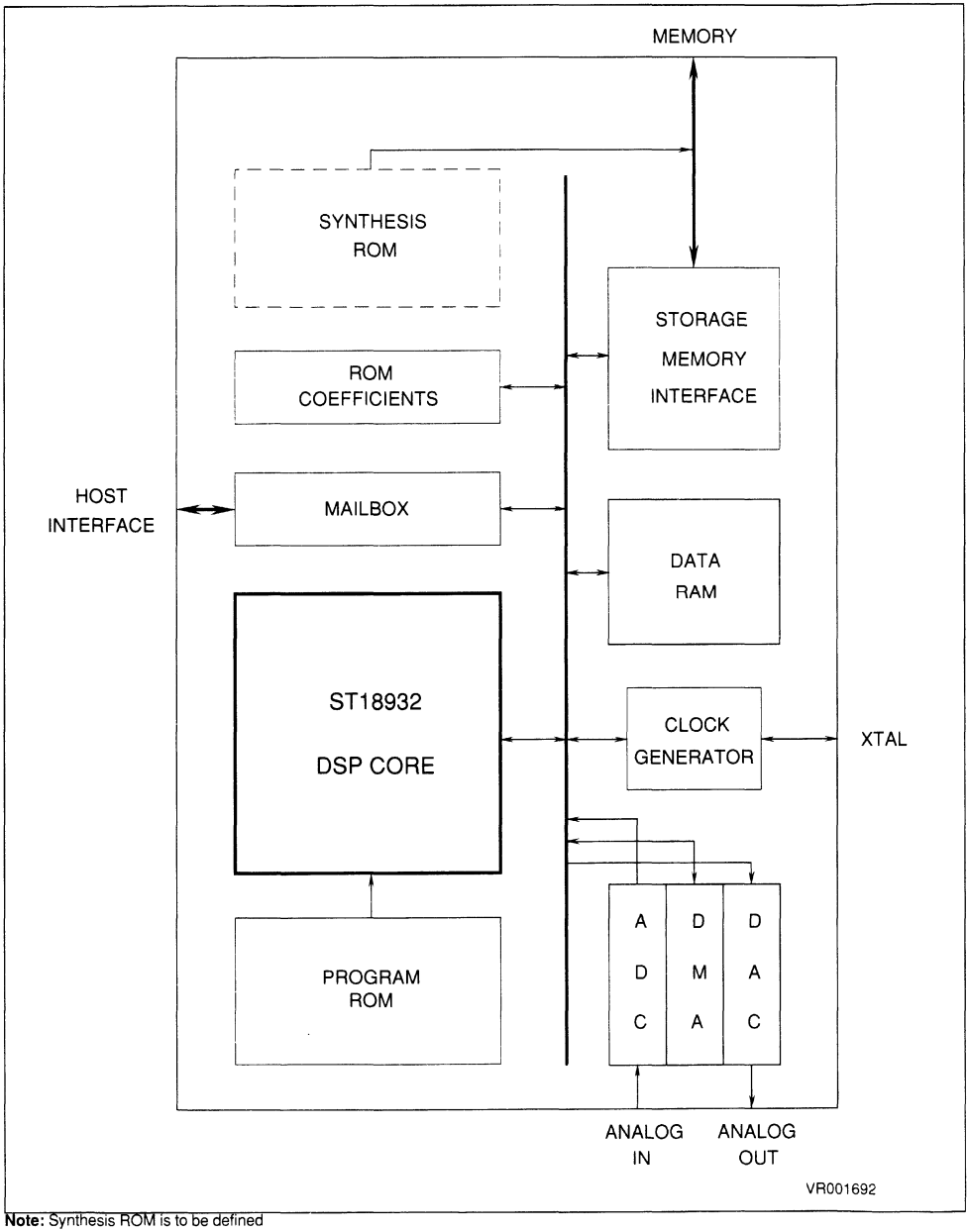
With respect to the signal received at the A/D converter input, the information provided by the ST18XSTAR is delayed by a processing time of 30 ms plus the transit time in the digital filters.

Reserved opcodes

The opcodes %11110000 to %11111111 are reserved.

6 APPENDIX

6.1 ST18XSTAR HARDWARE



Note: Synthesis ROM is to be defined

6.2 ELECTRICAL CHARACTERISTICS

Warning: *Following electrical characteristics and timings are related both to ST18XSTAR and ST18RXSTAR versions.*

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Note
V_{DD}	Supply Voltage	-0.3 to 7.0	V	2
V_{IN}	Input Voltage	-0.3 to 7.0	V	3
T_A	Operating Temperature Range	0 to 70	°C	
T_{STG}	StorageTemperature Range	-55 to 150	°C	
P_{DMAX}	Maximum Power Dissipation	1	W	
I_{OUT}	Analog Output Current	-200 to 200	µA	

Notes:

1. Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.
2. With respect to GND.
3. With respect to GND and with the condition $V_{IN} < V_{DD} + 0.5V$

DC Electrical Characteristics

(V_{DD} = 4.5V to 5.5V, T_A = 0 to 70°C)

Digital I/O Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{DD}	Supply Voltage	4.5	5.0	5.5	V	
V_{IL}	Input Low Level	-0.3	-	0.8	V	
V_{IH}	Input High Level (except EXTAL)	2.2	-	V_{DD}+0.3	V	
V_{IHE}	Input High Level (on EXTAL)	2.7	-	$V_{DD+0.3}$	V	
I_{IN}	Input Leakage Current (except EXTAL)	-10		+10	µA	1
I_{INEX}	Input Leakage Current on EXTAL			+20	µA	1
V_{OL}	Output Low Level (IOL = 1.6mA)	-	-	0.4	V	
V_{OH}	Output High Level (IOH = -400µA)	2.7	-	-	V	
I_{DD}	Supply Current (Full Operation 33MHz)		125		mA	3
I_{SB}	Stand-by Current (DRAM Refresh only)		1.5		mA	2,3
I_{TSI}	Three-State (Off State) Input Current	-20		+20	µA	
C_{IN}	Input Capacitance		10		pF	

Notes:

1. Test conditions: V_{IL} <= 0.4V; $V_{IH} = V_{DD}$
2. All inputs MUST be connected.
3. Relative to ST18XSTAR only

6.3 ANALOG I/O CHARACTERISTICS

Voltage References And Power Supply

Symbol	Parameter	Min.	Typ.	Max.	Unit
AV_{DD}	Supply Voltage	4.5	5.0	5.5	V
AV_{SS}	Ground		0		V
V_{CM}	Output Common Mode Voltage		2.5		V
V_{RH}	Output High Reference Voltage		3.75		V
V_{RL}	Output Low Reference Voltage		1.25		V
ABIAS	Input BIAS Control		50		µA

Rx Chain Characteristics (Measurement Band: DC to 3.4kHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{MS}	Input Maximum Swing		2.5		V_{PP}
R_{IN}	Input Resistance	100			kΩ
C_{IN}	Input Capacitance			20	pF
G_{ABS}	Absolute Gain at 1kHz	-0.5	0	0.5	dB
THD	Total Harmonic Distors. at -6dB,1kHz		-70		dB
SDR (1)	Signal Dynamic Range		80		dB
PSRR	Power Supply Rejection Ratio F=1kHz, V_{AC}=200mV_{PP}		40		dB

Note 1. Measurement made at -10dB

Tx Chain Characteristics

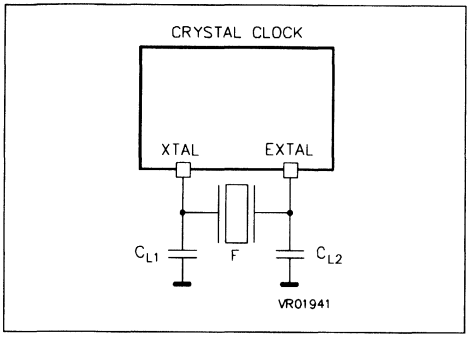
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OMS}	Output Maximum Swing		280		mV
ZL	Load Impedance	1			KΩ
IO	Output Current		200		µA
R_{OUT}	Output Resistance			10	Ω
V_{OFFOUT}	Output DC Offset	-100		+100	mV
A_{TT}	Absolute GAIN at 0dB Nominal Value		0		dB
RAT	Attenuation Relative to Nominal Value	-0.5		0.5	dB
THD	Total Harmonic Distors. at -6dB, 1kHz				dB
SDR	Signal Dynamic Range				dB
PSRR	Power Supply Rejection Ratio F=1kHz, V_{AC}=200mV_{PP}		40		dB

6.4 AC ELECTRICAL CHARACTERISTICS

Test Condition

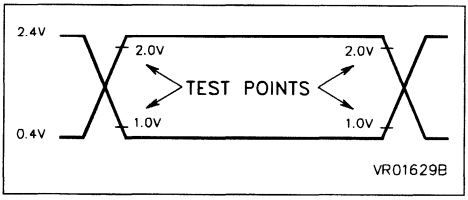
A crystal can be connected accross XTAL and EXTAL functioning in the parallel resonant fundamental mode, AT-cut.

Clock Connections



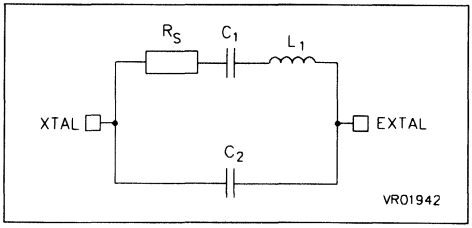
C_{L1},C_{L2} typical value = 10pF

AC Testing Input Output Waveform



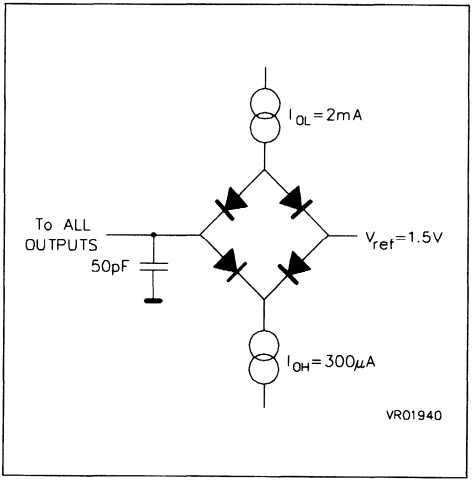
A.C. TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0" timing measurements are made at 2V for a logic "1" and at 1.0V for a logic "0".

Typical Crystal Equivalent Circuit



Typical values:: R_S = 10Ω
C1 = 0.02pF
C2 = 4pF
Q > 30k

AC Measurement Loads



6.5 CLOCK CHARACTERISTICS

A 4.096MHz crystal must be connected beetween XTAL and EXTAL to generate the pilot frequency for the ST18XSTAR clock generator.

This block generates the clock for :

- the ST18932 DSP core
- ADC and DAC converters
- the storage memory interface and the DRAMS refresh clock.

Symbol	Parameter	Min.	Typ.	Max.	Unit
FX	Main Oscillator Frequency EXTAL	-	4.096	-	MHz
1	EXTAL Cycle Time (T)	-	-	244	ns
3	EXTAL Rise and Fall Time		-	5	ns
4	PLL Start-up Time (1)	65.536T	-	-	ns

Note 1. Delay measured with a stabilized EXTAL signal when the ST18XSTAR is recovering from low-power mode

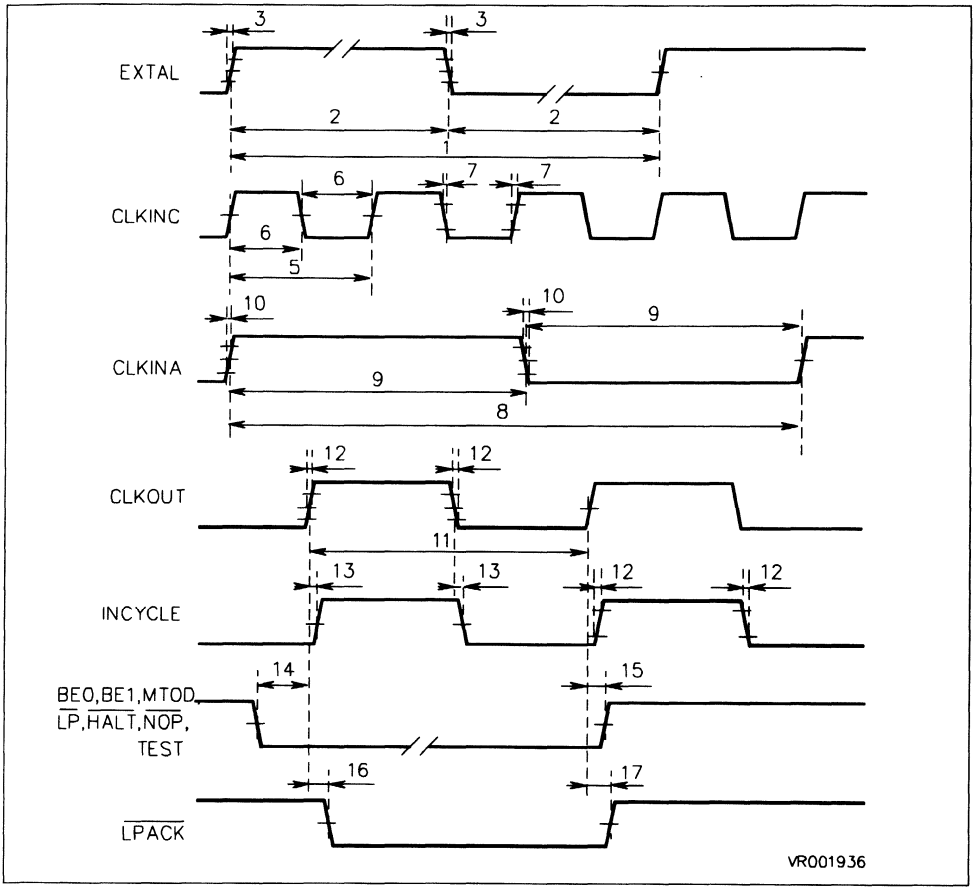
CLOCKS AND CONTROL SIGNALS

N°	Parameter	Min.	Max.	Unit
	EXTAL Frequency	4.096		MHz
1	EXTAL CYCLE TIME (T)		2.44	ns
2	EXTAL Pulse Width (f = 4.096MHz)			ns
3	EXTAL Rise and Fall Times		5	ns
4	PLL Start-up Time (1)	65.536T		ns
5	CLKINC (Input) Cycle Time	30	DC	ns
6	CLKINC (Input) Pulse Width	10		ns
7	CLKINC (Input) Rise and Fall Times		5	ns
8	CLKINA (Input) Cycle Time	30	40	ns
9	CLKINA (Input) Pulse Width	10		ns
10	CLKINA (Input) Rise and Fall Times		5	ns
11	CLKOUT Cycle Time (EXTAL = 4.096MHz)	60	DC	ns
12	CLKOUT Incycle Rise and Fall Times		5	ns
13	CLKOUT to Incycle delay	-5	+5	ns
14	BE0, BE1, MTOD, $\overline{LP}$, $\overline{HALT}$, $\overline{NOP}$ Set up Time	25		ns
15	BE0, BE1, MTOD, $\overline{LP}$, $\overline{HALT}$, $\overline{NOP}$ Hold Time	0		ns
16	CLKOUT High to $\overline{LPACK}$ Low Delay		25	ns
17	CLKOUT High to $\overline{LPACK}$ High Delay		15	ns

Note 1. This delay is measured with a stabilized EXTAL signal when the ST18XSTAR is recovering from low-power mode.

CLOCK CHARACTERISTICS (Continued)

AC Electrical Characteristics, Clocks And Control Signals

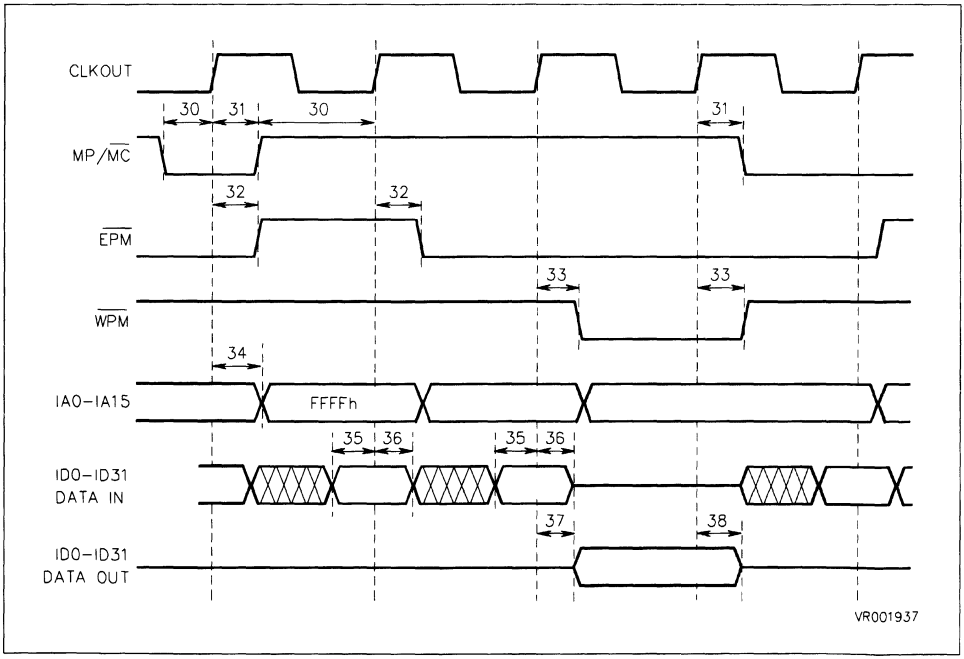


CLOCK CHARACTERISTICS (Continued)

Instruction Bus

N°	Parameter	Min.	Max.	Unit
30	MP/$\overline{MC}$ to CLKOUT Setup Time	20		ns
31	CLKOUT to MP/$\overline{MC}$ hold Time		5	ns
32	CLKOUT to $\overline{EPM}$ Delay		20	ns
33	CLKOUT to $\overline{WPM}$ Delay		20	ns
34	CLKOUT to Instruction Address Valid Delay		20	ns
35	DATA IN to CLKOUT Setup Time	20		ns
36	CLKOUT to DATA IN	5		ns
37	CLKOUT to DATA OUT Valid Delay		25	ns
38	CLKOUT to DATA OUT Hold Time	0		ns

AC Electrical Characteristics: Instruction Bus



CLOCK CHARACTERISTICS (Continued)

Storage Memory Interface

Values are given with:

- CLK = 4.096MHz (EXTAL)
- CLK Ratio = CLK High Level duration
- CLK Period = 40% to 60%

Switchings Characteristics For Dynamic Memories Accesses

N°	Parameter	Min.	Typ.	Unit
40	Read or Write Cycle		1	µs
41	$\overline{RAS0}$ (or 1) Low Pulse Duration		750	ns
42	$\overline{CAS}$ Low Pulse duration		500	ns
43	Delay Time. $\overline{RAS0}$ (or 1) Low to $\overline{CAS}$ Low	225		ns
44	Row-Address to $\overline{RAS0}$ (or 1) Setup Time (1)	75		ns
45	Row-Address Hold Time after $\overline{RAS0}$ (or 1) Low (1)	75		ns
46	Column-Address Setup Time before $\overline{CAS}$ Low (1)	75		ns
47	Column-Address Hold Time after $\overline{CAS}$ Low	225		ns
50	$\overline{MWE}$ Setup Time before $\overline{CAS}$ Low (1)	325		ns
51	$\overline{MWE}$ Hold Time after $\overline{CAS}$ and $\overline{RAS0}$ (or 1) high (1)	75		ns
52	WRITE. Data Setup Time (1)	325		ns
53	WRITE. Data Hold Time (1)	575		ns
60	CbR. $\overline{RAS0}$ (and 1) Low Pulse Duration (1)	575		ns
61	CbR. Delay Time $\overline{CAS}$ Low to $\overline{RAS0}$ (and 1) Low (1)	75		ns
62	CbR. Delay Time $\overline{RAS0}$ (and 1) Low to $\overline{CAS}$ High (1)	575		ns
63	CbR.$\overline{MWE}$ High Setup Time before $\overline{RAS0}$ (and 1) Low	225		ns
64	CbR.$\overline{MWE}$ High Hold Time after $\overline{RAS0}$ (and 1) Low	725		ns

Note 1. Parameter affected by the clock CLK ratio.
CbR means: CAS-before-RAS Refresh Cycle

Timing Requirement For Dynamic Memories Read Accesses

N°	Parameter	Min.	Typ.	Unit
54	Read. $\overline{CAS}$ to Output in Low-Z		225	ns
55	Read. Data Setup Time before $\overline{CAS}$ High	25		ns
56	Read. Data Hold Time after $\overline{CAS}$ High	0		ns
57	Read. Data Bus Release after $\overline{CAS}$ High		75	ns

CLOCK CHARACTERISTICS (Continued)

Switching Characteristics For Static Memories accesses

N°	Parameter	Min.	Typ.	Unit
70	Read or Write Cycle Duration		1	µs
71	MCS Low Pulse Duration		750	ns
72	Address and MWE Setup time before $\overline{MCS}$ Low (1)	75		ns
73	Address and $\overline{MWE}$ Hold time after $\overline{MCS}$ High	75		ns
74	WRITE. Data Setup Time	75		ns
75	WRITE. Data Hold Time	75		ns

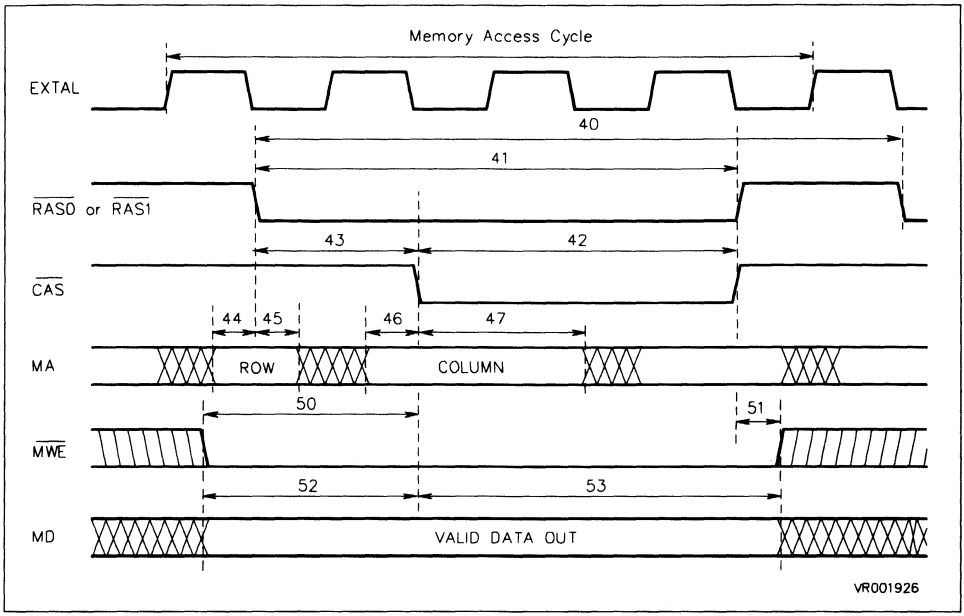
Note 1. Parameter affected by the clock CLK Ratio

Timing Requirement For Static Memories Read Accesses

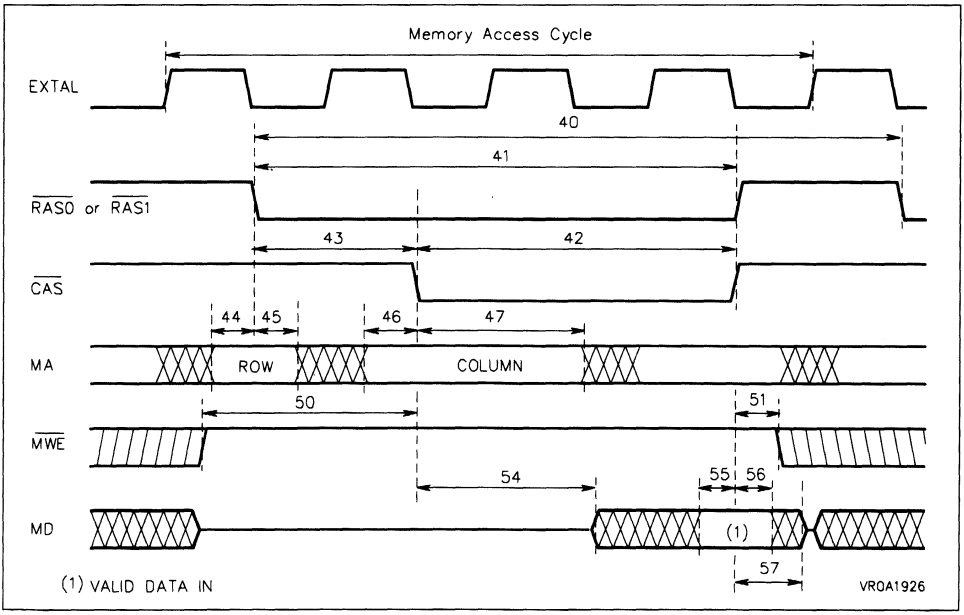
N°	Parameter	Min.	Typ.	Unit
76	Read. $\overline{MCS}$ to Output in Low-Z		475	ns
77	READ. Data Setup Time before $\overline{MCS}$ High	25		ns
78	READ. Data Hold Time after $\overline{MCS}$ High	0		ns
79	READ. Data Bus Release after $\overline{MCS}$ High		75	ns

CLOCK CHARACTERISTICS (Continued)

Dynamic Memories Write Cycle Timing

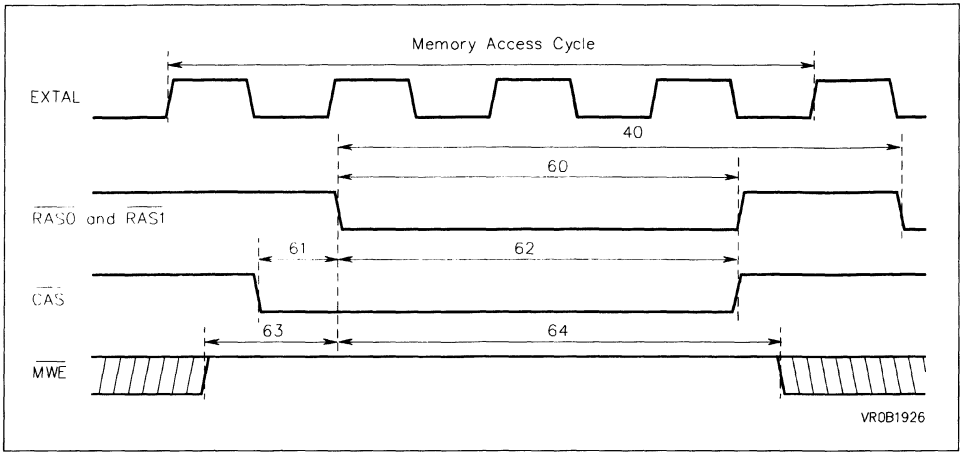


Dynamic Memories Read Cycle timing

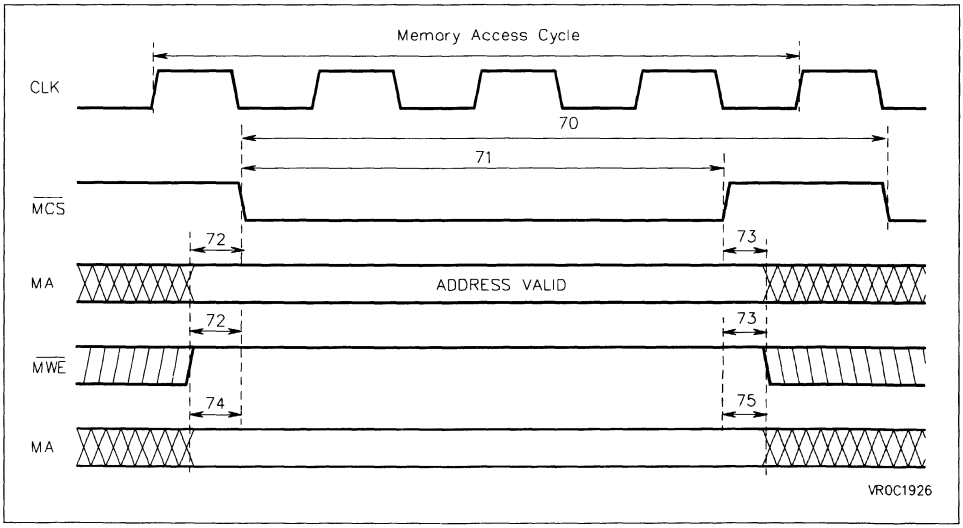


CLOCK CHARACTERISTICS (Continued)

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle

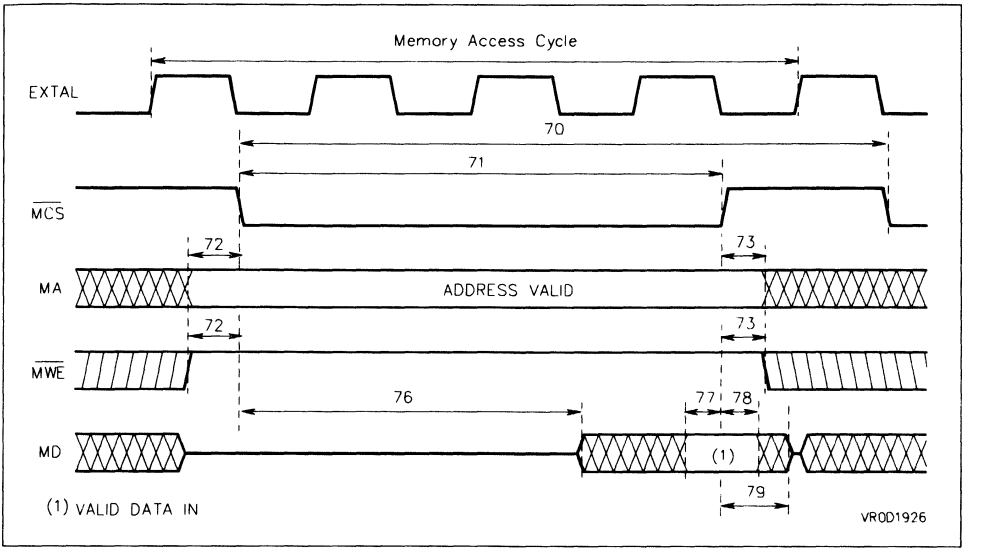


Static Memories Write Cycle Timing



CLOCK CHARACTERISTICS (Continued)

Static Memories Read Cycle Timing

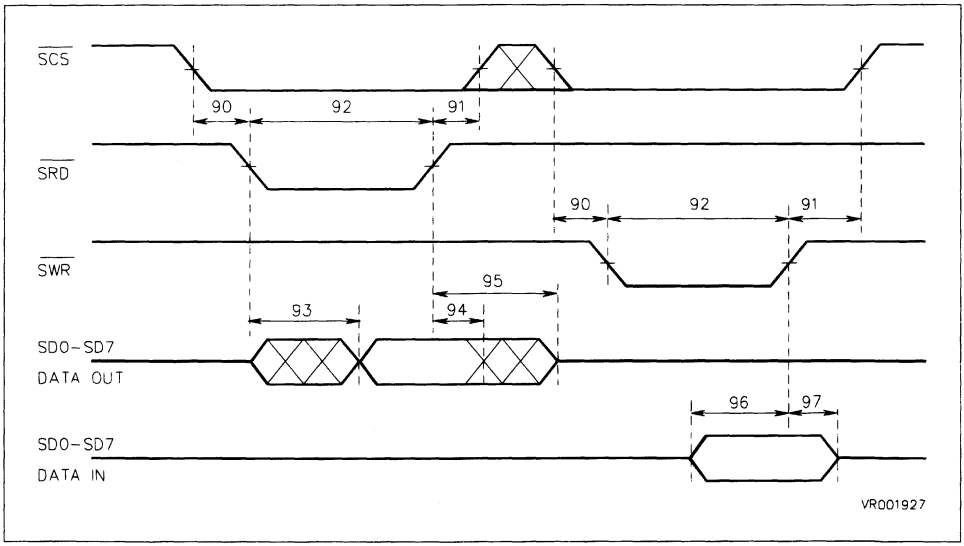


CLOCK CHARACTERISTICS (Continued)

Mailbox Interface

N°	Parameter	Min.	Max.	Unit
90	$\overline{SCS}$ to $\overline{SRD}$ and $\overline{SWR}$ Setup Time	10		ns
91	$\overline{SRD}$ and $\overline{SWR}$ to $\overline{SCS}$ Hold Time	10		ns
92	$\overline{SRD}$ and $\overline{SWR}$ Pulse Width	30		ns
93	$\overline{SRD}$ to SD0-SD7(Data Out) Delay		25	ns
94	$\overline{SRD}$ to SD0-SD7(Data Out) Hold Time	5		ns
95	$\overline{SRD}$ to SD0-SD7(Data Out) High Impedance		25	ns
96	SD0-SD7(Data In) to $\overline{SWR}$ Setup Time	15		ns
97	$\overline{SWR}$ to SD0-SD7(Data In) Hold Time	5		ns

AC Electrical Characteristics: Mailbox Interface

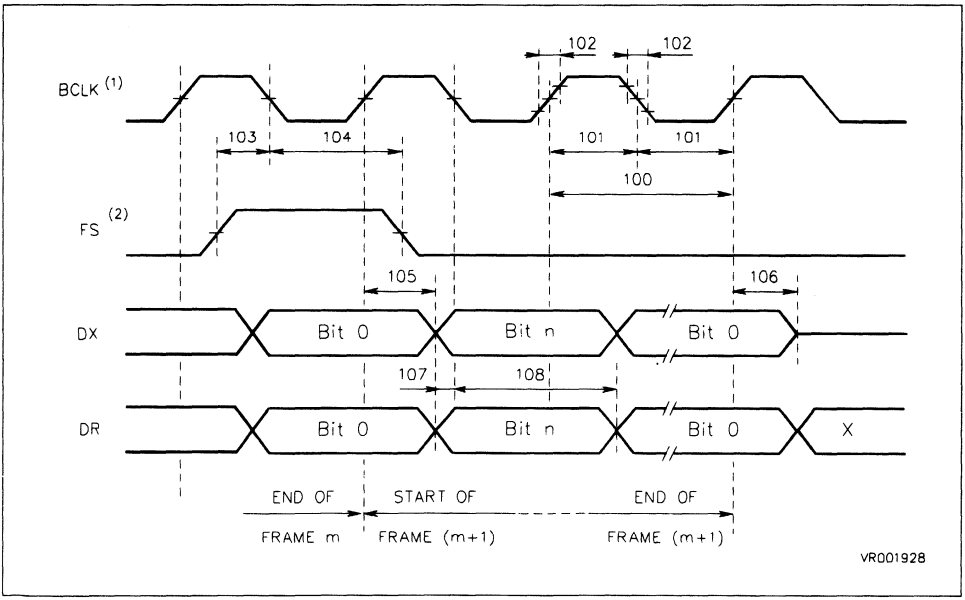


CLOCK CHARACTERISTICS (Continued)

Synchronous Serial Interface

N°	Parameter	Min.	Max.	Unit
100	BCLK Period	100		ns
101	BCLK Pulse Width	50		ns
102	BCLK Rise and Fall Times		30	ns
103	FS active to BCLK trailing edge Setup Time	20		ns
104	BCLK trailing edge to FS active Hold Time	5		ns
105	BCLK leading edge to DX valid delay		30	ns
106	BCLK leading edge to DX High Impedance		30	ns
107	DR to BCLK trailing edge Setup Time	20		ns
108	BCLK trailing edge to DR Hold TIme	10		ns

Serial Interface Timing



Notes:

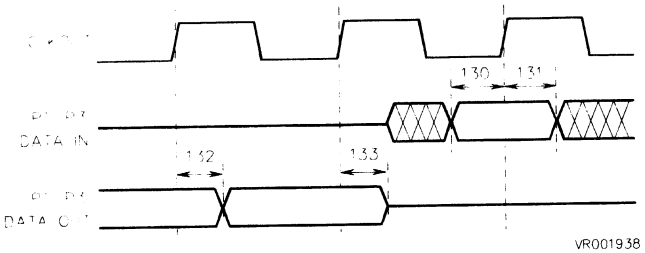
1. BCLK can be inverted, then the output data (DX) is transmitted on the falling edge of BCLK and the input data (DR) is sampled on the rising edge of BCLK.
2. FS can be a 1-bit or a half-Frame long pulse (positive or negative) in pulse modes operation.
   FS can be a high or low level, lasting for the whole frame of data in level modes operations.
3. When the SSI has the mastership of the bit clock and the frame synchro signals, the BCLK period depends on the DSP-CORE CLKOUT period and the SSI control register 3.

CLOCK CHARACTERISTICS (Continued)

Parallel Port

N	Parameter	Min.	Max.	Unit
130	P1.P3 Data In to CLKOUT Setup Time	25		ns
131	CLKOUT to P1.P3 (Data In) Hold Time	5		ns
132	CLKOUT to P1.P3 (Data Out) Delay		25	ns
133	CLKOUT to P1.P3 (Data Out) Hold Time	5		ns

AC Electrical Characteristics: Parallel Port

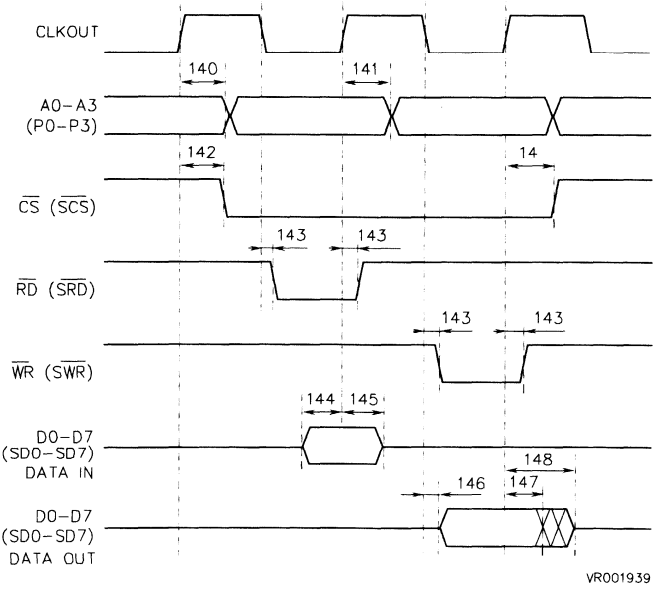


CLOCK CHARACTERISTICS (Continued)

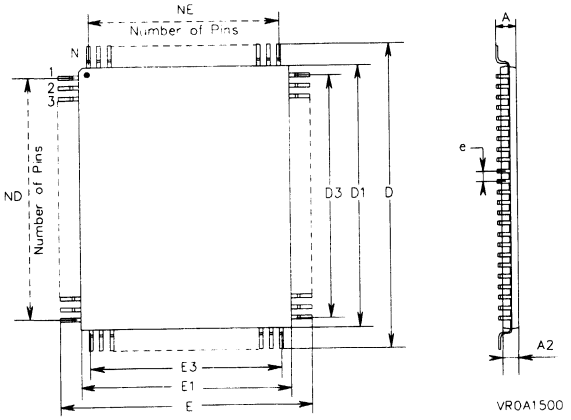
Data Bus In Debug/Emulation Mode (deb #2)

N°	Parameter	Min.	Max.	Unit
140	CLKOUT to ADDRESS Valid Delay		25	ns
141	CLKOUT to ADDRESS Hold Time	5		ns
142	CLKOUT to $\overline{CS}$ Delay		25	ns
143	CLKOUT to $\overline{RD}$,$\overline{WR}$ Delay	-5	+5	ns
144	DATA IN to CLKOUT Setup Time	15		ns
145	CLKOUT to DATA IN Hold Time	5		ns
146	CLKOUT to DATA OUT Valid Delay		25	ns
147	CLKOUT to DATA OUT Hold Time	5		ns
148	CLKOUT to DATA OUT High Impedance			ns

AC Electrical Characteristics: Data Bus In Debug/Emulation Mode (deb #2)



6.6 PACKAGE MECHANICAL DATA



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.30			0.130
A2	2.55	2.80	3.05	0.100	0.110	0.120
D	22.95	23.20	23.45	0.904	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.85			0.742	
E	16.95	17.20	17.45	0.647	0.667	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.35			0.486	
e		0.65			0.026	

Number of Pins	
N	100
ND	30
NE	20

SGS-THOMSON MICROELECTRONICS

ST18RXSTAR

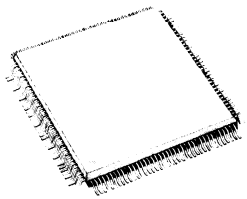
ROMLESS STATIC ANSWERING AND RECORDING CHIP

PRELIMINARY DATA

The ST18RXSTAR is the ROMless version of the ST18XSTAR.

The ST18XSTAR is a high quality low bit rate speech synthesis and recording system. Using ACELP type algorithms for voice compression at 4800bps. it offers the most competitive compromise between speech quality and memory size. It also includes voice synthesis capability, generated from a non volatile memory to produce predefined messages. Including tone and DTMF detectors for remote control operation. it is suitable for use in answering machines, answering telephone sets, cordless answering telephone sets.voice mail systems and memo recorders.

- Low bit rate (4.8kbps) speech coding and decoding system.
- Ultra low bit variable rate (<1.5kbps) speech synthesis message capability.
- Voice storage memory capability up to 32Mbits.
- Integrated implementation on one **D**igital **S**ignal **P**rocessor (DSP) chip.
- Low power design:
  - Single 5V power supply,
  - Maximum active power consumption 500mW,
  - Sleep power Mode 1.5mA for ARAM refresh.
- Reduced size and power consumption suitable for standard voice answering and recording machines, cordless phones with voice recording capability, memo recorders.
- Extended modes of operations and features :
  - Fast and slow read/skip modes. Messages monitoring.
  - Voice messages for remote operation through telephone line.
  - Possible use of SRAMs, DRAMs, ROMs or EPROMs.



PQFP160

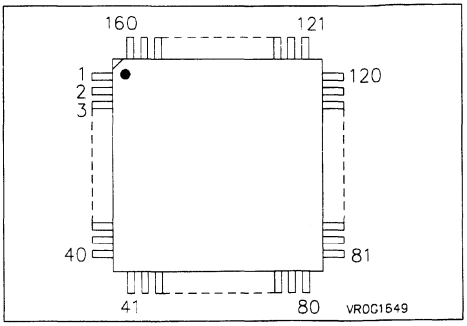
(Ordering information at the end of the datasheet)

  - Advanced error correction algorithms allowing use of ARAMs.
  - Programmable call progress and call waiting tone generators/detectors including DTMF,comply with PAA/TPA/AGH/1764 specifications.
  - Programmable voice activity detection for silence compression.
  - Programmable output attenuation level (for remote call screening).
  - Wide dynamic range (48dB).
  - PCM 64Kbps coding mode for high-quality incoming/outgoing messages.
- Versatile Interfaces
  - 3 to 1 muxed single-ended A/D input.
  - 2 D/A independently programmable output drivers.
  - On-chip converters.
  - Host processor parallel interface.

1 PIN DESCRIPTION

Warning: *This pinout is only related to ST18RXSTAR Emulation ROMless version.*

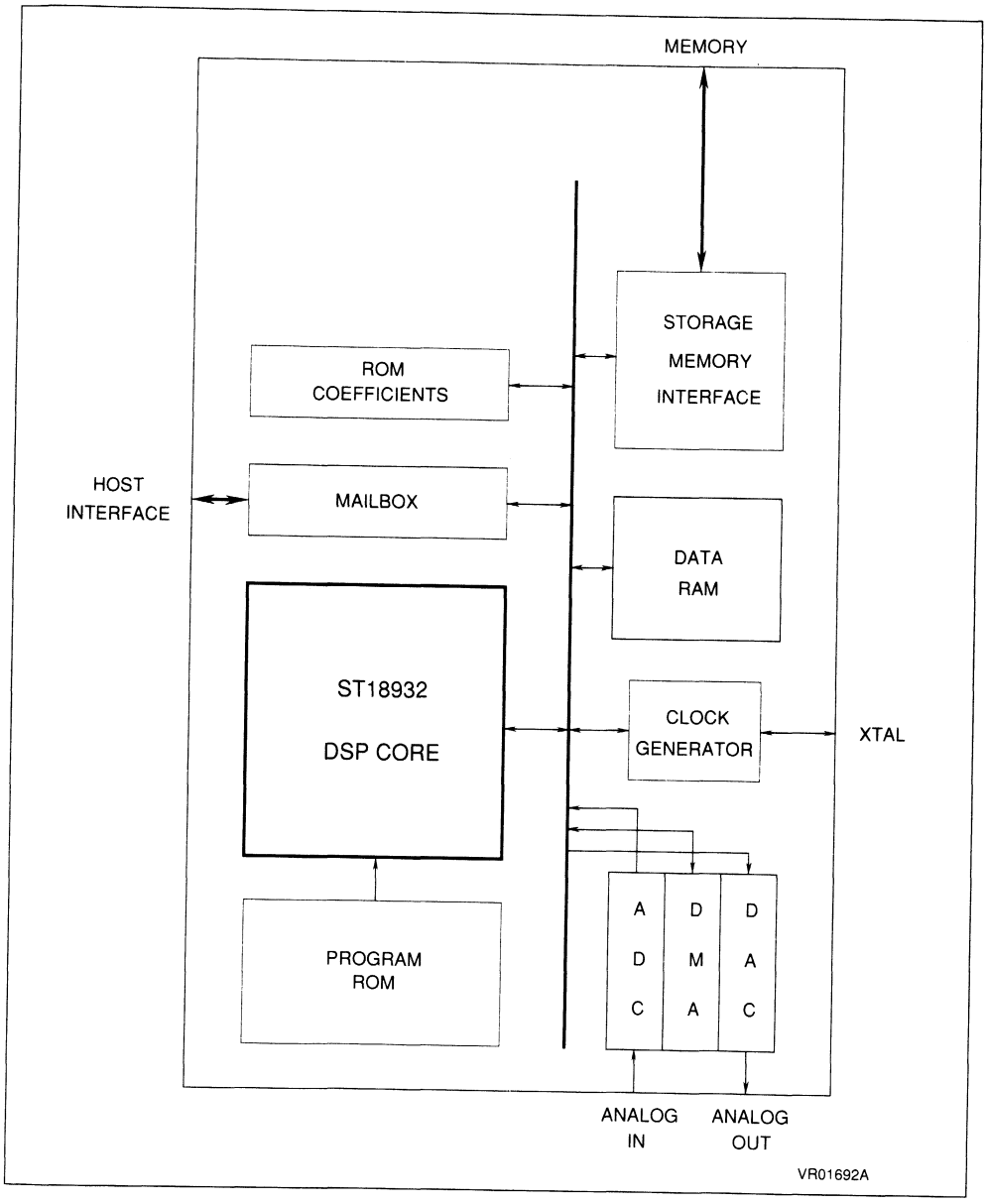
Figure 1. 160 Pin Quad Flat Pack (QFP) Package



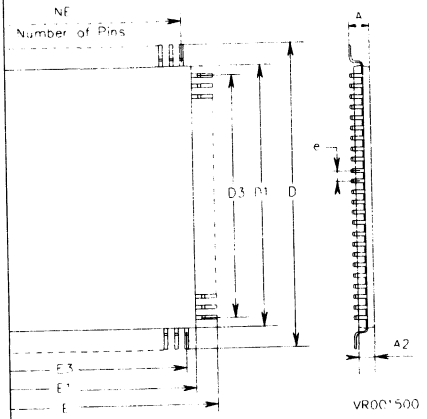
ST18RXSTAR (Emulation ROMless version) Pinout

Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	ID31	41	MCI	120	SD6	160	IA0
2	ID30	42	RDYS	119	SD7	159	IA1
3	ID29	43	MC2	118	DTOM	158	IA2
4	ID28	44	MC1	117	P1	157	IA3
5	ID27	45	MC0	116	P2	156	IA4
6	ID26	46	EOS	115	P3	155	IA5
7	ID25	47	BOS	114	V_{DD} PLL	154	IA6
8	ID24	48	SBACK	113	EXTAL	153	IA7
9	ID23	49	SCOUT	112	XTAL	152	IA8
10	ID22	50	V_{DD} PROM	111	CLKINC	151	IA9
11	ID21	51	$\overline{RAS1}$	110	CLKINA	150	IA10
12	ID20	52	$\overline{RAS0}$	109	V_{SS} PLL	149	IA11
13	ID19	53	$\overline{CAS}$	108	V_{SS} OUT	148	IA12
14	ID18	54	$\overline{MCS}$	107	INCYCLE	147	IA13
15	ID17	55	$\overline{MWE}$	106	LPACK	146	IA14
16	ID16	56	V_{DD} OUT	105	CLKOUT	145	V_{SS} RAM
17	ID15	57	V_{SS} OUT	104	LP	144	IA15
18	ID14	58	MA0	103	AV_{SS} ISO	143	V_{SS} OUT
19	ID13	59	MA1	102	ADIN0	142	V_{DD} OUT
20	V_{DD} IN	60	MA2	101	ADIN1	141	$\overline{MP/MC}$
21	V_{DD} RAM	61	MA3	100	ADIN2	140	$\overline{WPM}$
22	V_{SS} CLK	62	MA4	99	AV_{DD}	139	EPM
23	V_{DD} CORE	63	MA5	98	VCM	138	BE0
24	V_{SS} PROM	64	MA6	97	VRH	137	BE1
25	V_{SS} IN	65	MA7	96	VRL	136	MTOD
26	ID12	66	MA8	95	ABIAS	135	DX
27	ID11	67	MA9	94	AV_{SS} POL	134	DR
28	ID10	68	MA10	93	AV_{SS}	133	BCLK
29	ID9	69	MA11	92	DAOUT0	132	$\overline{FS}$
30	ID8	70	MA12	91	$\overline{DAOUT1}$	131	$\overline{SCS}$
31	ID7	71	MA13	90	$\overline{RESET}$	130	$\overline{SRD}$
32	ID6	72	V_{SS} CORE	89	$\overline{RESETC}$	129	$\overline{SWR}$
33	ID5	73	V_{DD} PERI	88	$\overline{TEST}$	128	V_{SS} IN
34	ID4	74	MA14	87	$\overline{HALT}$	127	V_{DD} IN
35	ID3	75	MA15	86	$\overline{NOP}$	126	SD0
36	ID2	76	MA16	85	V_{SS} PERI	125	SD1
37	ID1	77	MD0	84	MD7	124	SD2
38	ID0	78	MD1	83	MD6	123	SD3
39	SCIN	79	MD2	82	MD5	122	SD4
40	SCCLK	80	MD3	81	MD4	121	SD5

2 ST18RXSTAR HARDWARE



3 PACKAGE MECHANICAL DATA



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.90			.060
A2	3.10	3.40	3.65	.122	.134	.144
D	30.35	30.60	30.85	1.195	1.205	1.215
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		25.35			.998	
E	30.35	30.60	30.85	1.195	1.205	1.215
E1	27.90	28.00	28.10	1.098	1.102	1.106
E3		25.35			.998	
e		0.65			.026	
Number of Pins						
N	160					
ND	40					
NF	40					